EPSON®

EQUITY II+

Personal Computer

SERVICE MANUAL

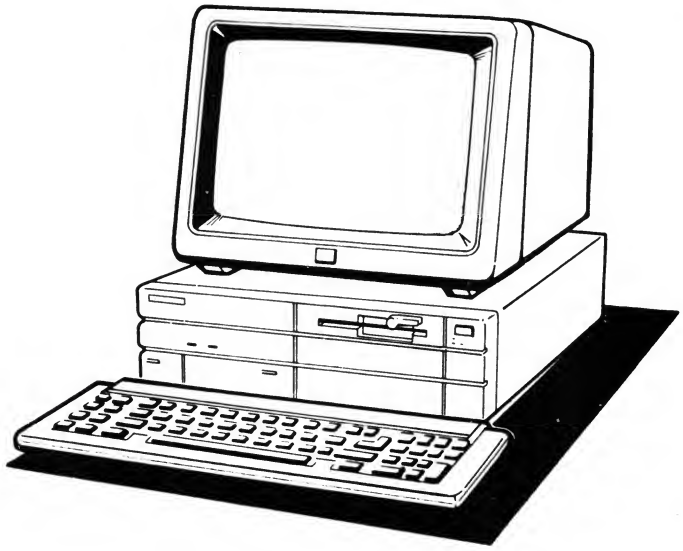
EPSON AMERICA, INC.

Mary Lou Young

EPSON
SERVICE DIVISION

EQUITY II+

TECHNICAL MANUAL



Seiko Epson Corporation
Nagano, Japan

Y16299900200

FCC COMPLIANCE STATEMENT

This equipment uses and generates radio frequency energy and it not installed and used properly, that is in strict accordance with the manufacture's instructions, may cause interference to radio and television reception.

It has been type tested and found to comply with limits for a Class B computing device in accordance with Sub – part J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment dose cause interference to radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- reorient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer away from the receiver
- plug the computer into a different outlet so that the computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet, prepared by the Federal Communications Commission, helpful:
"How to Identify and Resolve Radio – TV interference Problems. "This booklet is available from the U.S. Government Printing Office, Washington. D.C., 20402, Stock No. 044 – 000 – 00345 – 4.

You can determine whether your computer is causing interference by turning it off. If the interference stops, it was probably caused by the computer or its peripheral devices. To further isolate the problem, disconnect either the peripheral device or its I/O cable.

These devices usually require shielded cable. For Epson peripheral devices, you can obtain the proper shielded cable from your dealer. For non – Epson devices, contact the manufacturer or dealer for assistance.

Seiko Epson Corporation, Nagano, Japan

PRECAUTIONS

Precautionary notations throughout the text are categorized relative to 1) personal injury and 2) damage to equipment.

DANGER Signals a precaution which, if ignored, could result in serious or fatal personal injury. Great caution should be exercised in performing procedures preceded by DANGER Headings.

WARNING Signals a precaution which, if ignored, could result in damage to equipment.

The precautionary measures itemized below should always be observed when performing repair/ maintenance procedures.

DANGER

1. ALWAYS DISCONNECT THE PRODUCT FROM BOTH THE POWER SOURCE AND PERIPHERAL DEVICES PERFORMING ANY MAINTENANCE OR REPAIR PROCEDURE.

2. NO WORD SHOULD BE PERFORMED ON THE UNIT BY PERSONS UNFAMILIAR WITH BASIC SAFETY MEASURES AS DICTATED FOR ALL ELECTRONICS TECHNICIANS IN THEIR LINE OF WORK.

3. WHEN PERFORMING TESTING AS DICTATED WITHIN THIS MANUAL, DO NOT CONNECT THE UNIT TO A POWER SOURCE UNTIL IN-STRUCTED TO DO SO. WHEN THE POWER SUPPLY CABLE MUST BE CONNECTED, USE EXTREME CAUTION IN WORKING ON POWER SUPPLY AND OTHER ELECTRONIC COMPONENTS.

WARNING

1. Repairs on Epson product should be performed only by an Epson certified repair technician.

2. Make certain that the source voltage is the same as the rated voltage, listed on the serial number/rating plate. If the Epson product has a primary AC rating different from available power source, do not connect it to the power source.

3. Always verify that the Epson product has been disconnected from the power source before removing or replacing printed circuit boards and/or individual chips.

4. In order to protect sensitive microprocessors and circuitry, use static discharge equipment, such as anti-static wrist straps, when accessing internal components.

5. Replace malfunctioning components only with those components by the manufacture; introduction of second-source ICs or other non-approved components may damage the product and void any applicable Epson warranty.

REVISION	ISSUE DATE	REVISION PAGE
REV.A	September 1987	-

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Subsequent product modifications will be brought to your attention via Service Bulletins; please revise the text as bulletins are received.

This document is subject to change without notice.

CHAPTER 1

PRODUCT DESCRIPTION

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1.1 FEATURES

The Epson EQUITY II+ / PC AX2 is a small footprint, high-performance, 80286-based desktop microcomputer providing complete hardware and software compatibility with the IBM(R) PC AT(R).

1.1.1 SYSTEM FEATURES

The system features include:

Two hardware-switchable operating speeds, 8MHz and 10MHz,

Expansion bus interface for 16-bit and 8-bit expansion boards,

Two jumper-selectable Numeric Processor Extension (NPX) clock speeds,

Independently-selectable wait-state options for system ROM and expansion I/O devices,

BIOS support for a wide range of Hard Disk Drives including those recently supported by the IBM PS/2(R) line,

Floppy Disk Controller,

Parallel Interface,

9-pin Asynchronous Serial RS232C Interface,

International Power Supply

1.2MB Floppy Disk Drive

640KB of RAM

The Epson EQUITY II+ / PC AX2 Enhanced Model also contains a Hard Disk Controller and a 20MB or 40MB Hard Disk Drive.

1.1.2 HARDWARE CONFIGURATION

The Epson Equity II+ / PC AX2, in its standard configuration, is composed of the main unit and the keyboard. The main unit contains the system board, Epson Multi-Function board (serial, parallel and floppy disk controllers), international power supply, one 1.2MB floppy disk drive, and the expansion board connectors.

In addition to the standard 1.2MB floppy disk drive (FDD) are two floppy disk drive options available: a 720KB 3.5" micro-floppy disk drive, and a 360KB 5.25" mini-floppy disk drive.

There are three optional hard disk drive (HDD) configurations. The factory-installed HDD option provides a Seiko Epson (Model HMD-720) 20MB half-height HDD with a 69ms average access time. The second HDD option is a Tokico (Model TD5046) 40MB half-height HDD with a 40ms average access time. The third HDD option is a Control Data (Model 94205-51) 40MB half-height HDD with an average access time of 28ms.

Video options include a Monochrome Display Adapter, Color Graphics Adapter, Multi-function Graphics Adapter (including Hercules(TM)-compatible monochrome graphics, monochrome text and color graphics capabilities), and an EGA-compatible video board.

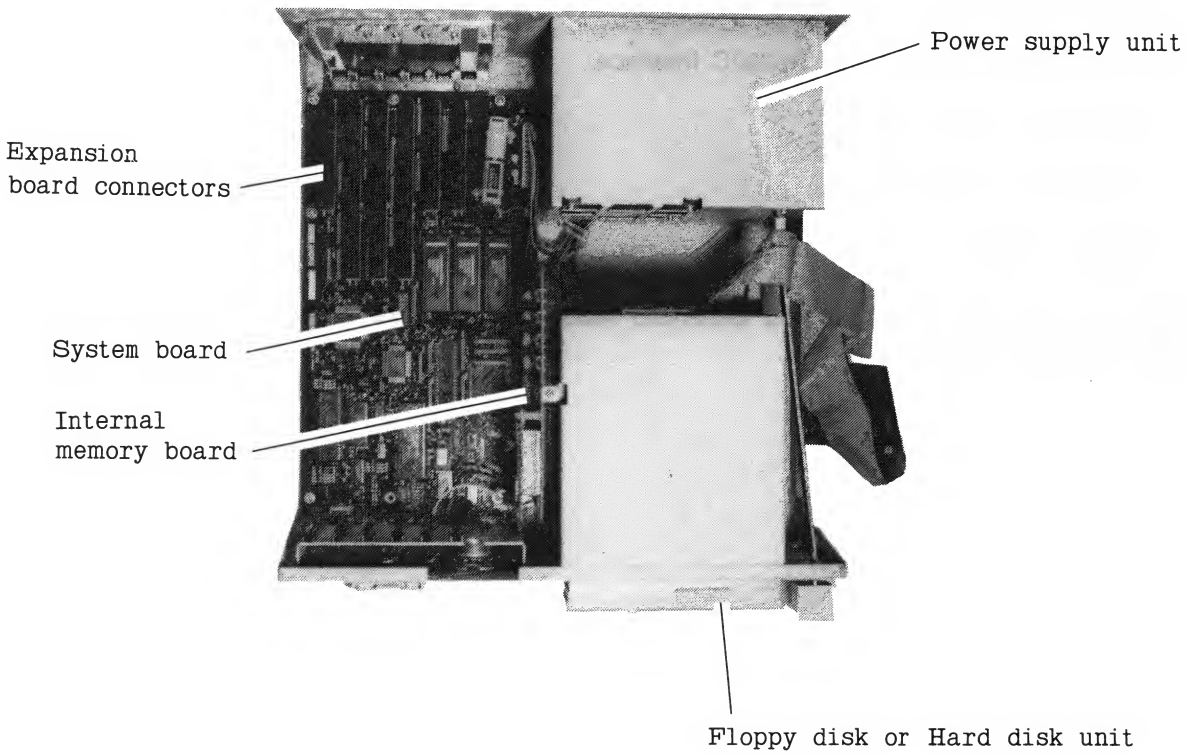

FIGURE 1-1. MAIN UNIT COMPONENT LOCATIONS

1.2 SPECIFICATIONS

The following specifications apply to the complete system. Specifications for each of the major subassemblies follow this section.

POWER SUPPLY		
Input Voltage (Switchable)		
U.S.		
Rated	115V AC	
Valid	95V – 137V AC	
Europe		
Rated	230V	
Valid	195V – 265V AC	
Frequency, Valid	47Hz – 63Hz	
Power Consumption	110W Typical, 140W Max.	
Inrush Current	32A or less, for 1/2 Cycle, Maximum	
Output		
12V	+12V : 4.5A	–12V : 0.3A
5V	+5V : 10A	–5V : 0.3A
INSULATION STRENGTH		
Primary – Secondary	1,500V AC for 1 minute	
Primary – Frame Ground	1,500V AC for 1 minute	
Secondary – Frame Ground	500V AC for 1 minute	
INSULATION RESISTANCE		
Primary – Secondary	50MΩ Min. (500V DC)	
Secondary – Frame Ground	50MΩ Min. (500V DC)	
Secondary – Frame Ground	50MΩ Min. (500V DC)	

MAXIMUM ENVIRONMENTAL CONDITIONS	*Operating*	*Non – Operating*
Ambient Temperature	5°c to 35°c	–20°c to 60°c
Humidity		
Relative (non – condensing)	20% to 80%	10% to 90%
Wet Bulb		
Standard Model	29°c	40°c
Enhanced Model	26°c	29°c
Altitude (atmospheric pressure)		
Standard Model	0m to 10,000m	0m to 10,000m
Enhanced Model	0m to 3,000m	0m to 10,000m
SHOCK RESISTANCE, MAXIMUM	1G, 10ms	3G, 10ms
VIBRATION RESISTANCE, MAXIMUM		
Standard Model	0.2G, 5 to 150Hz	1G, 5 to 150Hz
Enhanced Model	0.2G, 5 to 150Hz	0.5G, 5 to 150Hz

1.2.1 MAIN UNIT SPECIFICATIONS

DIMENSIONS	
Height	6.10" (155mm)
Width	15.75" (400mm)
Depth	16.26" (413mm)
Weight (1 FDD Model)	19.8lbs. (9 Kg)
MICROPROCESSOR	80286
COPROCESSOR (Optional)	80287 – 8
BASIC INPUT/OUTPUT SYSTEM (BIOS)	AT – compatible: 2 128K – bit EPROM chips
SYSTEM CLOCK SPEED	10MHz or 8MHz (hardware switchable)
SYSTEM SUPPORT CHIPS	T4758 – Includes functions of: 2 Direct Memory Access Controllers (DMAC) (Intel 8237A – 5 compatible) 2 Interrupt Controllers, (INTC) (Intel 8259A compatible) 1 Timer/Counter (Intel 8254 – 2 compatible)
Seiko Epson AT – Chipset	Custom gate arrays providing: data – and address – bus control; system clock and timing control; memory address, refresh, and timing generation; miscellaneous system support circuitry.
KEYBOARD INTERFACE	8042 – based Enhanced (101/102 – key) Keyboard – compatible Interface, plug – compatible with IBM Enhanced or Standard PC AT Keyboard.
SERIAL COMMUNICATIONS INTERFACE	RS – 232C serial interface (9 – pin D – shell)
PARALLEL INTERFACE	Centronics – compatible parallel printer interface
EXPANSION BUS INTERFACE	3 8 – bit PC – compatible expansion slots (1 used by Multi – Function card, 2 open) 3 16 – bit AT – compatible expansion slots (Enhanced Model: 1 used for HDC, 2 open)
MASS STORAGE SLOTS	3 Half – height drive bays. (May be configured by user as 1 full – height and 1 half – height.)
MASS STORAGE	
Standard Model	1 5.25" high – density double – sided floppy disk drive (1.2MB formatted capacity)
Enhanced Model	1 5.25" 1.2MB floppy disk drive (same as above) One of the following: 1 Half – height 3.5" 20MB 65ms Hard Disk Drive 1 Half – height 5.25" 40MB 28ms Hard Disk Drive 1 Half – height 5.25" 40MB 40ms Hard Disk Drive

TABLE 1-1. ANDRO BOARD COMPONENT DESCRIPTION

Name	*Model*	*Location*	*Function*
CPU	80286-10	6C	16 bit CPU
NPX	80287-8	5C	Co-processor (socket only)
Super Integration Chip	T4758	1B	DMA control, Interrupt control, counter/timer
RTC	146818	2D	System clock, calender and CMOS RAM
KEYBOARD I/F	8042	1D	Interface between 80286 and keyboard
GAATAB	E01085CB	6A	Controls CPU address bus (A16-0), system address bus (SA16-0) and internal address bus (XA16-0). Generates refresh address.
GAATCB	E01086CA	4A	Control bus (I/O write pulse, I/O read pulse, memory write pulse, memory read pulse) and 7 MSB of address bus (A23-17) and bus high enable signal.
GAATDB	E01068CA	5A	Control CPU bus (D15-0), system data bus (SD15-0) and memory data bus (MD15-0)
GAATCK	E01068CA	4D	Clock generator, bus controller and shut down circuit.
GAATCX	E01117BA	5D	Clock generator, Clock selector
GAATRF	E01069BB	6D	Controls D-RAM refresh, DMA transfer, 16-8 data bit conversion, and wait state insertion.
GAATIO	E01092EA	3C	Address decoder for I/O space and I/O registers.

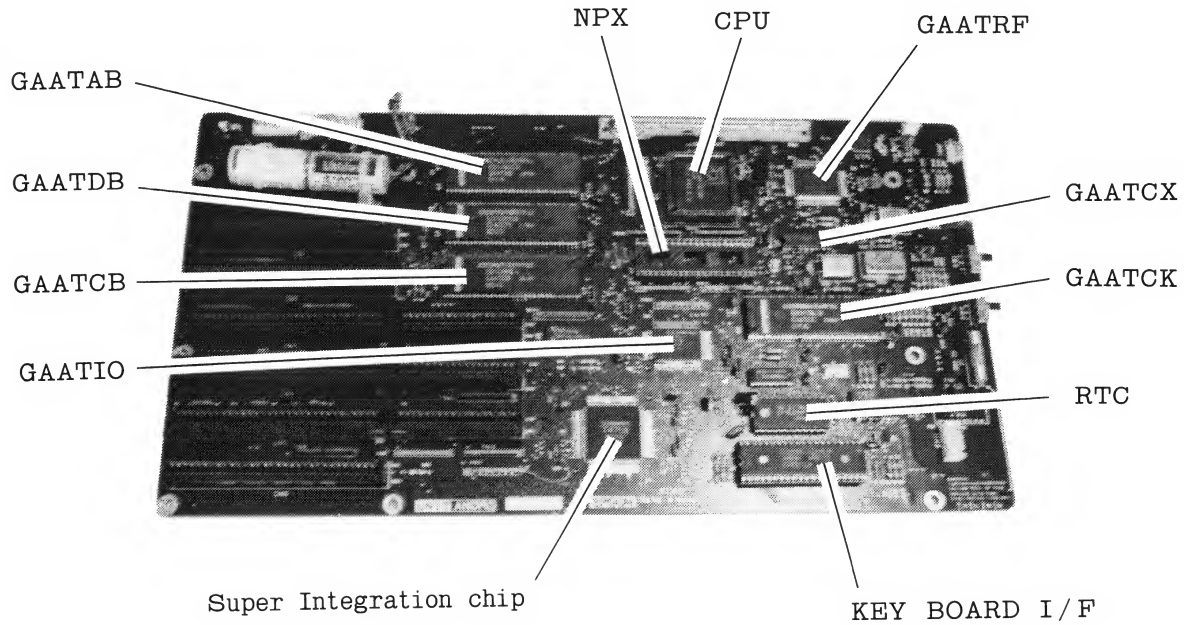

FIGURE 1-2. COMPONENT LOCATIONS ON MAIN CONTROL BOARD

1.2.2 KEYBOARD SPECIFICATIONS

LAYOUT	101 – key (102 in Europe) "Enhanced" keyboard
CORD	60cm (23.6") 5 – wire, coiled, unshielded cable
STATUS INDICATORS	LED indicators, controlled by commands from the Main Unit, for "Num Lock" "Scroll Lock" and "Caps Lock".
CONNECTOR	Main Unit end: 5 – pin, "O" – shell (IBM plug compatible) Keyboard end: 5 – wire "modular" cable jack (Epson proprietary)
WEIGHT	3.02lbs (1.37Kg)
DIMENSIONS	Width: 19.3" (49cm) Depth: 7.8" (19.75cm) Height: 1.9" (4.77cm)

1.2.3 FLOPPY DISK DRIVE SPECIFICATIONS

1.2.3.1 1.2MB FLOPPY DISK DRIVE SPECIFICATIONS

MODEL NUMBER	NEC model FD1155C, FD1157C; Cannon MD5501		
CAPACITY	1.2MB Formatted; 1.6MB Unformatted;		
DATA TRANSFER RATE	500Kbps Max.; 300Kbps optional.		
STEP RATE (Track – to – track seek)	3ms		
HEAD SETTLE TIME	15ms, Minimum		
HEAD LOADING TIME	35ms, Minimum		
MOTOR START TIME	800ms, Minimum		
MOTOR SPEED	360 rpm		
CYLINDERS	80		
TRACKS	160 (80 cylinders x 2 heads)		
CURRENT REQUIREMENTS	*At "Motor On"*		*Typical*
+12V	390mA		210mA
+5V	460mA		460mA
POWER CONSUMPTION	4.8 Watts		
DIMENSIONS	Width:	5.75"	(14.6cm)
	Depth:	8"	(20.3cm)
	Height:	1.61"	(4.1cm)
ENVIRONMENTAL CONDITIONS	*Operating*		*Non – Operating*
Temperature	4° to 46°c		– 20° to 65°c
Relative Humidity (non – condensing)	20% to 80%		10% to 90%
Temperature Change (per hour)	15°c		30°c
Vibration (x, y or z axis)	100Hz		100Hz
Shock(x, y or z axis)	10G		15G

1.2.3.2 720KB 3.5" FLOPPY DISK DRIVE (OPTIONAL)

MODEL NUMBER	Seiko Epson SMD – 489M	
CAPACITY	720KB Formatted; 1000KB Unformatted	
DATA TRANSFER RATE	250Kbps	
DATA ACCESS TIME	100ms, average	
STEP RATE (Track – to – track seek)	3ms	
HEAD SETTLE TIME	15ms	
HEAD LOADING TIME	15ms	
MOTOR START TIME	500ms	
MOTOR SPEED	300rpm	
CYLINDERS	80	
TRACKS	160 (80 x 2 heads)	
CURRENT REQUIREMENTS	*Reading*	*Maximum*
+5V	360mA	1.0A
POWER CONSUMPTION	1.8W	
DIMENSIONS	Width: 4.0" (10.2cm)	
	Depth: 5.9" (15.0cm)	
	Height: 1.0" (25.4cm)	
	Weight: 1.3 lbs. (585g)	
ENVIRONMENTAL CONDITIONS	*Operating*	*Non – Operating*
Temperature	4°c to 45°c	–20°c to 65°c
Relative Humidity (non – condensing)	20% to 80%	95% maximum
Vibration (x, y or z axis)	5 to 500Hz, 0.6G	5 to 500Hz, 3G
Shock(x, y or z axis)	5G	50G

1.2.3.3 360K 5.25" FLOPPY DISK DRIVE (OPTIONAL)

MODEL NUMBER	Cannon MD5201		
CAPACITY	Formatted: 360KB; Unformatted: 500KB		
DATA TRANSFER RATE	250KB/sec		
STEP RATE (Track-to-track seek)	6ms		
HEAD SETTLE TIME	15ms		
HEAD LOADING TIME	95ms		
MOTOR START TIME	500ms		
MOTOR SPEED	300rpm		
CYLINDERS	40		
TRACKS	80 (40/side)		
CURRENT REQUIREMENTS	*Peak*	*Typical*	*Maximum*
+12V	1.310A	250mA	460mA
+5V	-	140mA	180mA
POWER CONSUMPTION (Typical)	*Reading*	*Writing*	*Waiting*
	2.75W	3.61W	0.87W
DIMENSIONS	Width: 5.8" (14.8cm)		
	Depth: 7.8" (19.8cm)		
	Height: 1.7" (4.2cm)		
ENVIRONMENTAL CONDITIONS	*Operating*		*Non-Operating*
Temperature	5°c to 45°c		-22°c to 60°c
Relative Humidity (non-condensing)	20% to 80%		10% to 90%
Vibration	< 1G, 10Hz to 100Hz		< 3G, 10Hz to 100Hz
Shock	< 5G		< 50G

1.2.4 HARD DISK DRIVE SPECIFICATIONS

1.2.4.1 20MB HALF-HEIGHT HARD DISK DRIVE (OPTIONAL)

MODEL NUMBER	Seiko Epson HMD-720	
CAPACITY	20MB Formatted; 25.5MB Unformatted	
DATA TRANSFER RATE	5Mbps	
DATA ACCESS TIME	69ms, average (includes Head Settle Time)	
STEP RATE (Track-to-track seek)	18ms, average (includes Head Settle Time)	
CYLINDERS	615	
TRACKS	2460 (615 x 4 heads)	
SECTORS/TRACK	32	
MOTOR SPEED	3,528 rpm (±01%)	
INTERFACE	ST-506/412	
CURRENT REQUIREMENTS	*Average*	*Maximum*
+12V	580mA	770mA
+5V	200mA	360mA
POWER CONSUMPTION	8.0 Watts	
DIMENSIONS	Width: 5.8" (14.6cm)	
	Depth: 7.8" (19.8cm)	
	Height: 1.6" (4.1cm)	
	Weight: 2.7 lbs (1.23Kg)	
ENVIRONMENTAL CONDITIONS	*Operating*	*Non-Operating*
Temperature	4° to 50°c	-40° to 65°c
Relative Humidity (non-condensing)	8% to 85%	8% to 85%
Altitude (atmospheric pressure)	3,000m	10,000m
Vibration	5 to 36Hz: 0.15mm	5 to 12Hz: 10.2mm
	36 to 500Hz: 0.4G	13 to 500Hz: 3.0G
Shock	8G, 10ms	40G, 10ms

1.2.4.2 40MB HALF – HEIGHT 28MS HARD DISK DRIVE (OPTIONAL)

MODEL NUMBER	CDC 94205 – 51
CAPACITY	42MB Formatted; 50.24MB Unformatted
DATA TRANSFER RATE	5Mbps
DATA ACCESS TIME	28ms, average (includes Head Settle Time
STEP RATE (Track – to – track seek)	5ms, average (includes Head Settle Time)
MOTOR SPEED	3,597rpm (±0.5%)
HEADS	5
CYLINDERS	989
TRACKS	4,945 (989 x 5 sides)

CURRENT REQUIREMENTS	*Typical*	*Maximum*	*Start – up*
+12V	1.5A	2.0A	4.5A
+5V	400mA	600mA	1.0A

POWER CONSUMPTION	20 Watts
DIMENSIONS	Width: 5.75" (14.60cm) Depth: 8.1" (20.57cm) Height: 1.625" (4.13cm) Weight: 3.8 lbs. (1.73Kg)

ENVIRONMENTAL CONDITIONS	*Operating*	*Non – Operating*
Temperature	10° to 50°c	14° to 130°c
Relative Humidity (non – condensing)	8% to 80%	8% to 90%
Temperature Change (per hour)	10°c	20°c
Vibration (x, y or z axis)	5 to 22Hz, 0.5mm 22 to 500Hz, 0.5G Max.	5 to 22Hz, 0.5mm 22 to 500Hz, 0.75G Max.
Shock (x, y or z axis)	2G, 10ms Max.	40G, 10ms Max.

1.2.4.3 40MB HALF-HEIGHT 40MS HARD DISK DRIVE (OPTIONAL)

MODEL NUMBER	Tokico TD 5046
CAPACITY	40.3MB Formatted; 50.92 Unformatted
DATA TRANSFER RATE	5Mbps
STEP RATE (Track-to-track seek)	8ms
DATA ACCESS TIME	40ms Average (includes Head Settle Time)
MOTOR SPEED	y3,550rpm
CYLINDERS	615
TRACKS	4920 (615 x 8)
HEADS	8

CURRENT REQUIREMENTS	*Typical*	*Power-On*
+12V	1.8A	3.5A
+5V	1A	-

POWER CONSUMPTION	26.6 Watts		
DIMENSIONS	Width:	5.87"	(14.9cm)
	Depth:	8.19"	(20.8cm)
	Height:	1.69"	(4.3cm)
	Weight:	4lbs.	(1.8Kg)

ENVIRONMENTAL CONDITIONS	*Operating*	*Non-Operating*
Temperature	5° to 45°c	-20° to 60°c
Temperature Change (per hour)	10°c/h	10°c/h
Relative Humidity (non-condensing)	5% to 80%	5% to 90%
Vibration (x, y or z axis)	0.25G Max.	2G Max.
Shock(x, y or z axis)	2G Max.	20G Max.

CHAPTER 2

PRINCIPLES OF OPERATION

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2.1 SYSTEM OVERVIEW

Figure 2 – 1 shows the interconnection of the main CPU unit, floppy disk drives, the keyboard, and the monitor. Pin assignments for each connector are detailed in Appendix.

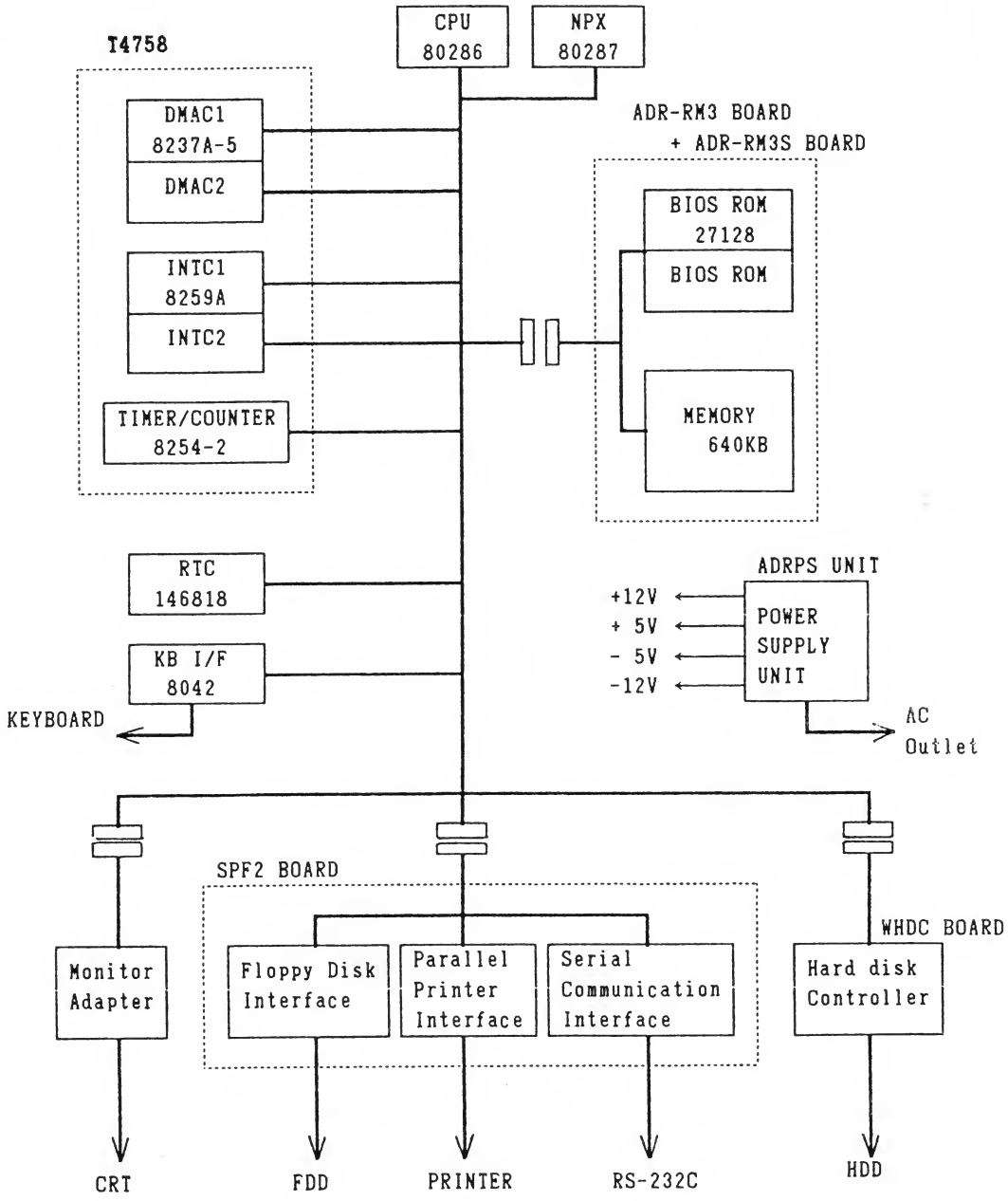


FIGURE 2 – 1. SYSTEM CONFIGURATION BLOCK DIAGRAM

2.2 ADRPS POWER SUPPLY UNIT

The EQUITY II+ / EPSON PC AX2 power supply, simply called the ADRPS unit is a switching power supply of the ringing choke converter (RCC) type. It produces four DC voltages +5V, −5V, +12V, and −12V from the 115V or 230V input. The unit conforms to safety standards UL478, CSA C−22, 2−154, and TUV; and noise standards FCC class B, and FTZ class B. It is housed in a light alloy case and positioned on the right at the rear of the main unit. The unit supplies power to the system board, adapter board, FDD, HDD, K/B, and monochromatic CRT.

The power supply has a voltage doubler rectification circuit that can switch the input voltage range to either 115 − 120V or 220 − 240V, 50/60Hz, so that it can be used anywhere in the world. The input voltage can be switched to either 115V AC or 230V AC by the two position slide switch on the rear panel.

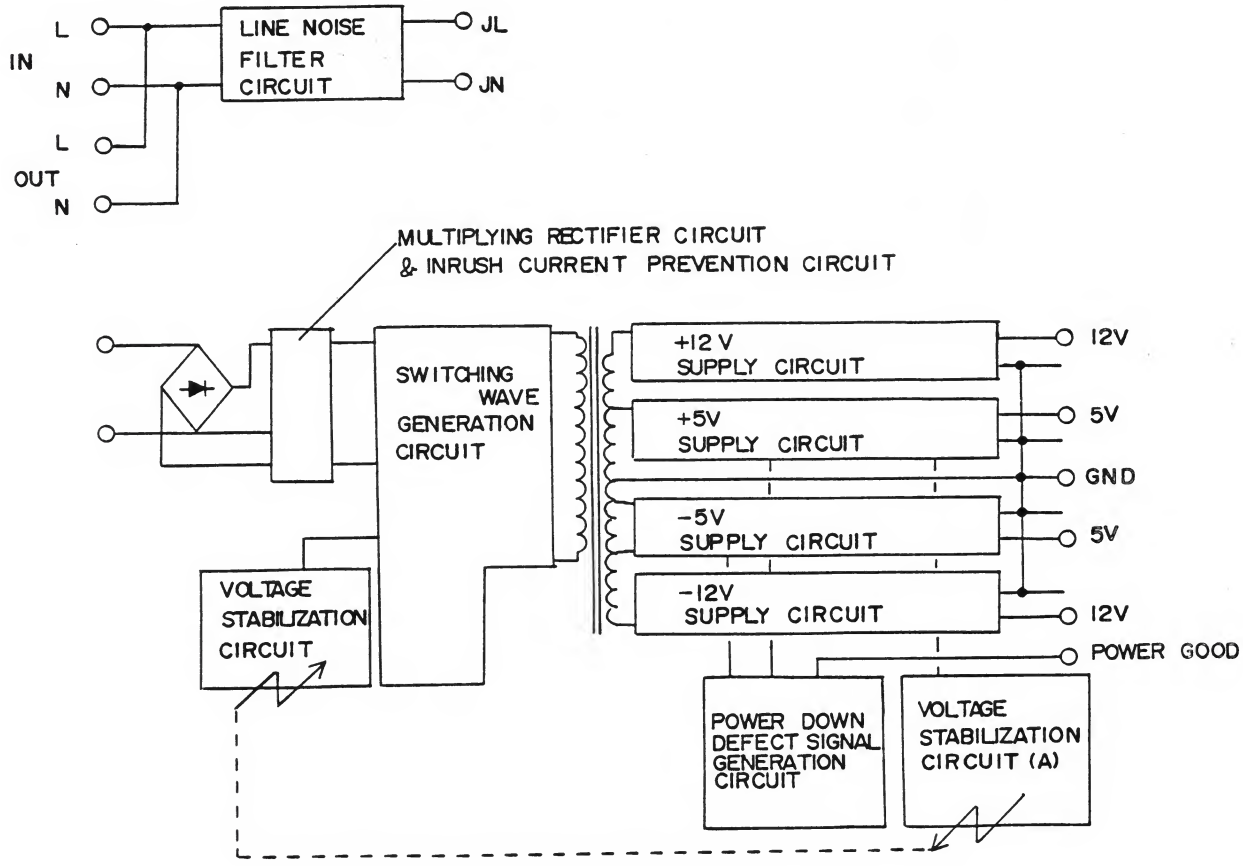


FIGURE 2−2. POWER SUPPLY DIAGRAM

AC OUTPUT RATING

The unit has an AC output socket that supplies a maximum output current of 1A to an optional external device, such as a CRT.

DC OUTPUT RATING

Table 2-1 shows the DC output ratings.

TABLE 2-1. DC OUTPUT RATINGS

BASIS GROUND OF VOLTAGE	GL	GP	GL	GL
RATED OUTPUT VOLTAGE	+5 V	+12 V	-12 V	-5 V
RATED OUTPUT CURRENT	10 A	4.5 A	0.3 A	0.3 A
MINIMUM OUTPUT CURRENT	1.0 A	0 A	0 A	0 A
REGULATION	+-5%	+-5%	+-10%	+-10%
RIPPLE	50 mVpp	100 mVpp	100 mVpp	50 mVpp
RIPPLE + NOISE	100 mVpp	200 mVpp	200 mVpp	100 mVpp
OVERCURRENT PROTECTION	YES	YES	YES	YES
OVERVOLTAGE PROTECTION	YES	NO	NO	NO

2.2.1 PRIMARY-SIDE CIRCUITS

2.2.1.1 AC VOLTAGE INPUT SELECTION CIRCUIT

The user can select the AC input voltage by setting the two position slide switch (SW2) on the rear of the unit to either 115V or 230V. The unit supplies current to the circuit appropriate to the input voltage selected by SW2; the fuse, voltage doubler rectification circuit, and surge current prevention circuit for the 115V AC input are different from those for the 230V AC input. In a 110V AC system, current flows through fuse F1, and in a 230V AC system, it flows through fuse F2. (See figure 2-1) The voltage doubler rectification circuit and surge current prevention circuit are described below.

2.2.1.2 LINE – NOISE FILTER CIRCUIT

The line – noise filter circuit prevents malfunction due to input surge voltage or input return noise. C1, C2, C3, and R1 C4 remove normal – mode noise; L1, L2, C5, and C6 remove common – mode noise. Figure 2 – 1 shows the line – noise filter circuit.

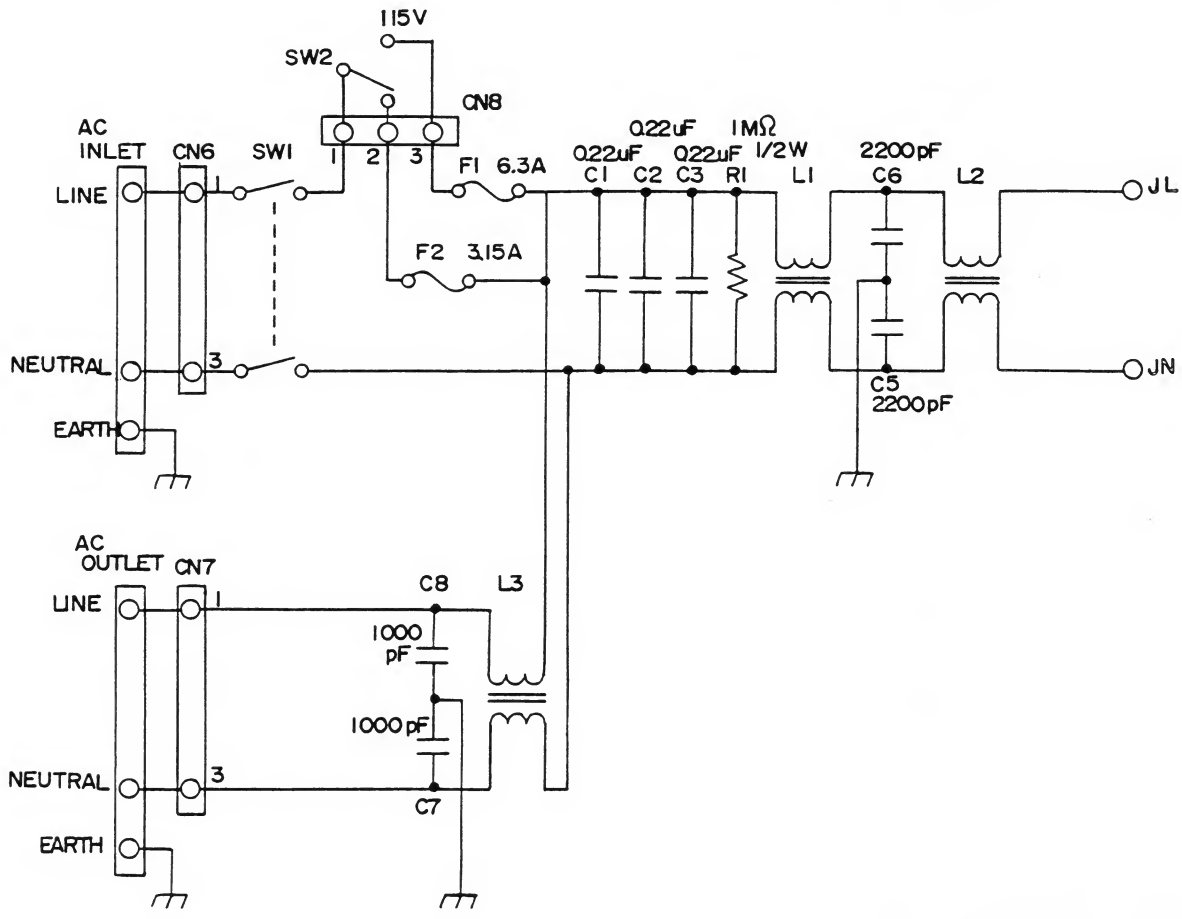


FIGURE 2 – 3. LINE NOISE FILTER CIRCUIT

2.2.1.3 VOLTAGE RECTIFICATION AND SURGE PREVENTION CIRCUIT

The voltage doubler rectification circuit and surge current prevention circuit differ according to the AC input voltage. The voltage doubler rectification circuit rectifies the 115V AC voltage to produce 230V AC. It consists of D1, C11, and C12. The surge current prevention circuit prevents a large current from flowing into the rectifying capacitor when power is turned on and protects components. This circuit contains TH11 and TH12. SW2 is closed when the input voltage is 115V AC. A positive half cycle input through the AC line conducts D1 – 1, buffers surge current by TH11, charges C11 to the maximum voltage, and flows to the neutral side through SW2. The negative half cycle that follows induces current from the neutral side. The current passing through SW2 charges C12 to the same voltage as C11 in the same direction, then

flows to the line through TH12. Thus, a DC current with twice the AC input voltage is obtained for the system. SW2 is open when the AC input voltage is 230V AC, and therefore, normal bridge rectification is performed. Figure 2-2 shows the voltage doubler rectification circuit and surge current prevention circuit.

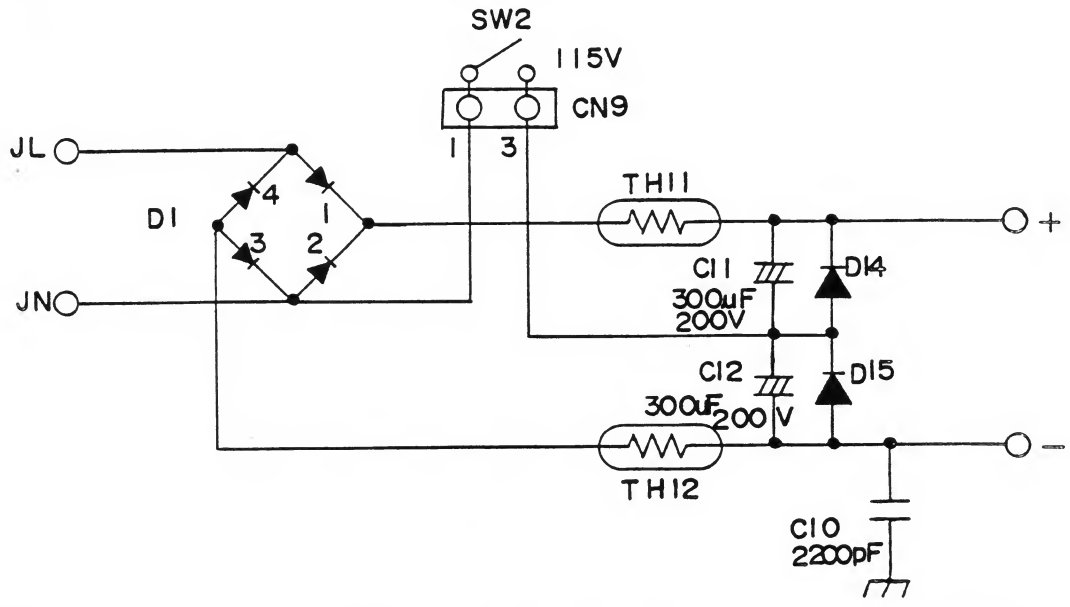


Figure 2-4. VOLTAGE DOUBLER RECTIFIER CIRCUIT

2.2.1.4 SWITCHING-WAVE GENERATION CIRCUIT

The offline switching IC, IC11 (STK7408), generates switching pulses with a frequency of 33KHz and drives the primary side of the pulse transformer PT1. The PT1 primary winding NP1 is used to drive the secondary side, and Np2 returns excess current from the secondary side load to the primary side. D13, C16, R16a and R16b form a snubber circuit that buffers the spike voltage that occurs on switching off. The circuit consisting of ZD11, ZD12, and TR11 is the soft start overshooting. Figure 2-3 shows the switching wave generation circuit.

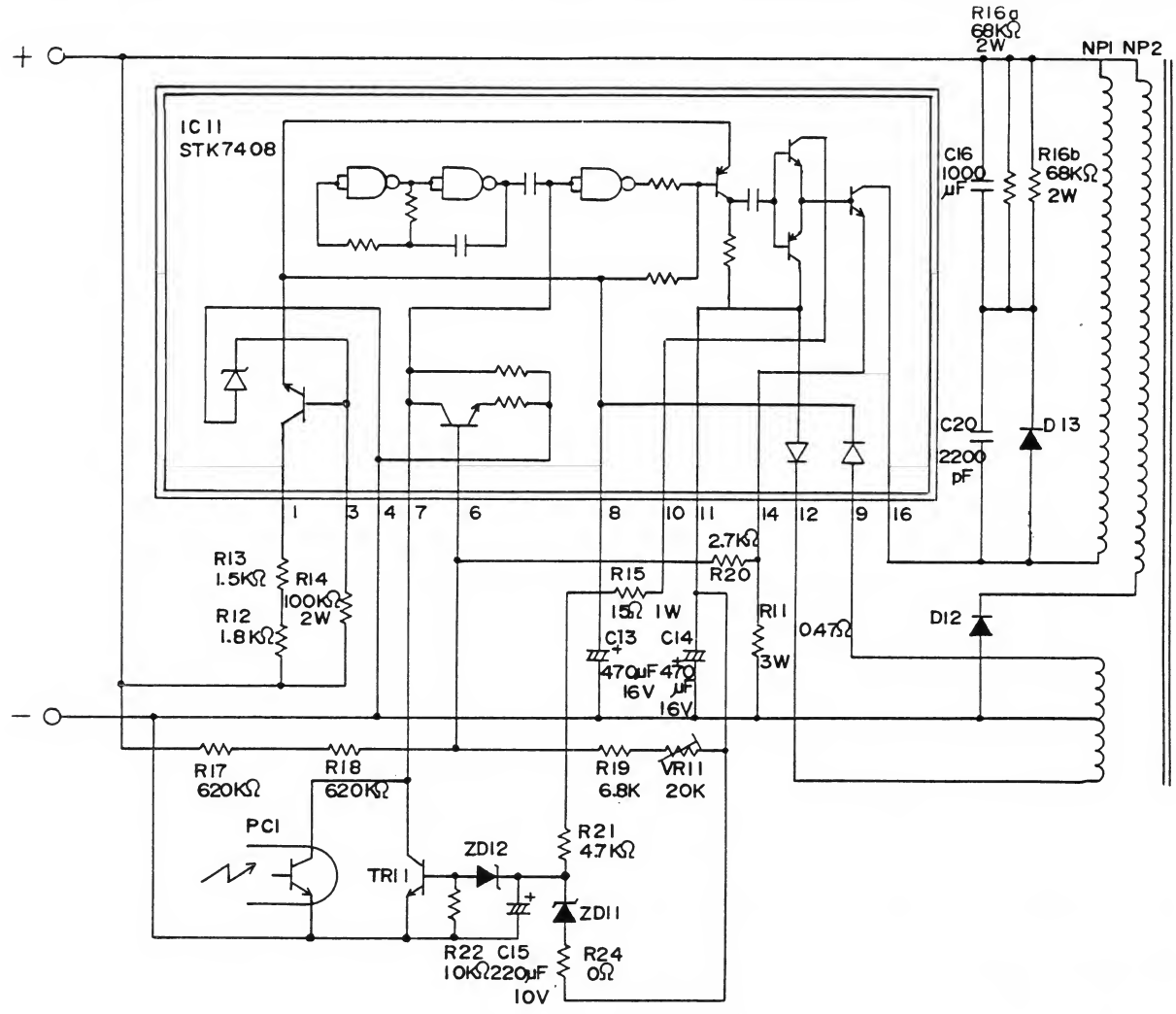


FIGURE 2-5. SWITCHING WAVE GENERATION CIRCUIT

2.2.2 SECONDARY-SIDE CIRCUIT

2.2.2.1 +12V SUPPLY CIRCUIT

When the primary side switching is OFF, an electro-motive force (EMF) is produced in PT1 in the direction of (1), and the current is rectified by D32 and supplied by charging C35 and C36.

When the primary side switching is On, an EMF is generated in PT1 in the direction of (2) and the current is supplied by discharging C35 and C36. C57 and C53 prevent the spike voltage.

This circuit is a dropper-type stabilizing power supply containing voltage regulator IC3 (78MG) and TR31. R54 and TR35 detect overcurrent, turn TR34 on, and decrease the TR31 collector current by controlling IC31 input. ZD33 forms a clover overvoltage protection circuit by

connecting the anode to the SCR31 gate. R32 and R33 detect the reference voltage and stabilize the voltage by controlling IC31. Figure 2-6 shows the +12V supply circuit.

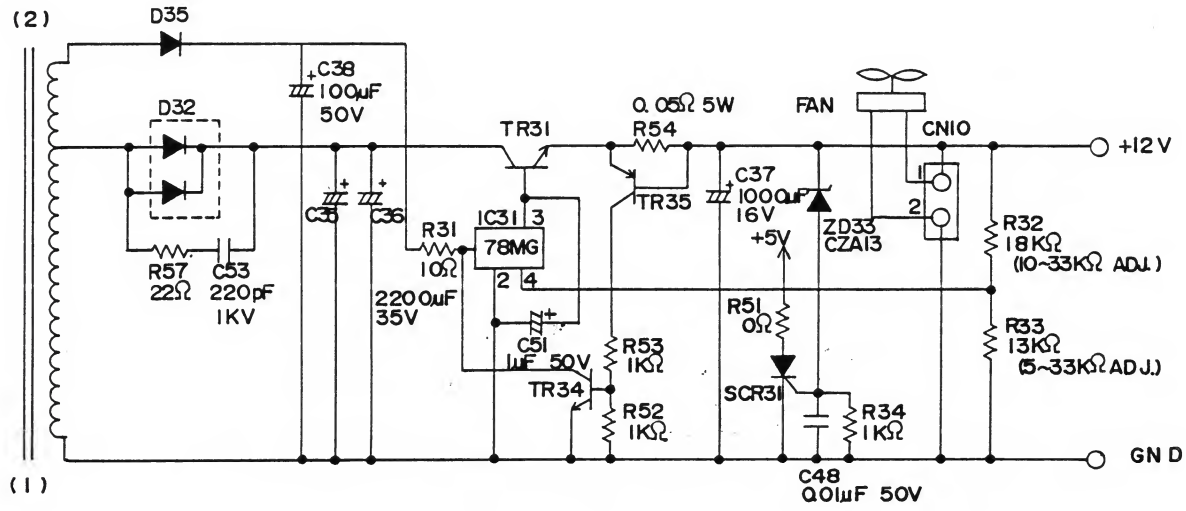


FIGURE 2-6. +12V SUPPLY CIRCUIT

2.2.2.2 +5V SUPPLY CIRCUIT

The basic operations of the +5V supply circuit are the same as those of the +12V DC supply circuit described above. L31 removes ripples; ZD32 and SCR31 form a clover overvoltage protection circuit. Figure 2-7 shows the +5V supply circuit.

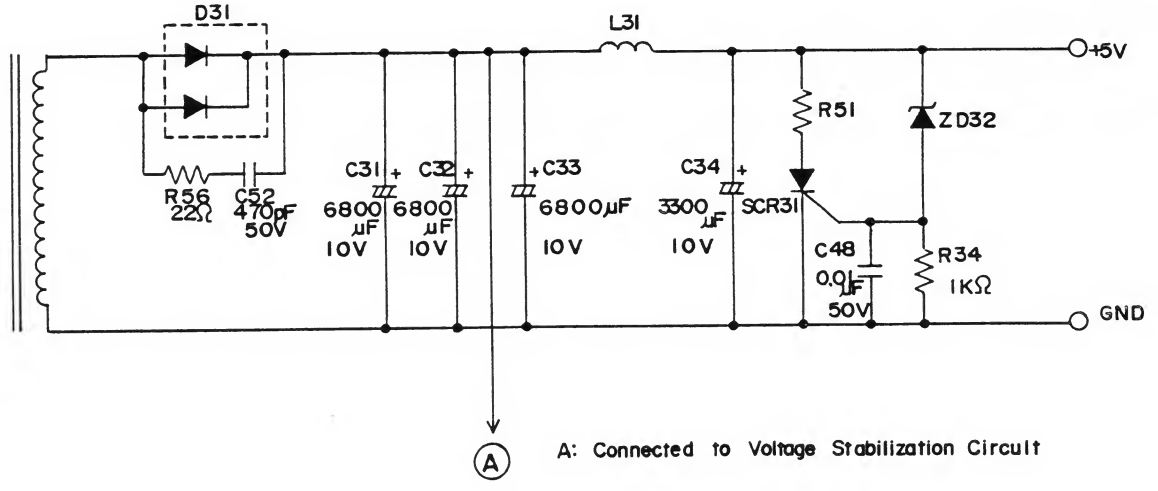


Figure 2-7. +5V SUPPLY CIRCUIT

2.2.2.3 −5V / −12V SUPPLY CIRCUIT

The basic operations of the −5V / −12V supply circuit are the same as those of the +12V supply circuit. −5V DC is generated and supplied by IC32 (79M05). −12V DC is generated and supplied by IC33 (79M12). Figure 2−8 shows the −5V / −12V supply circuit.

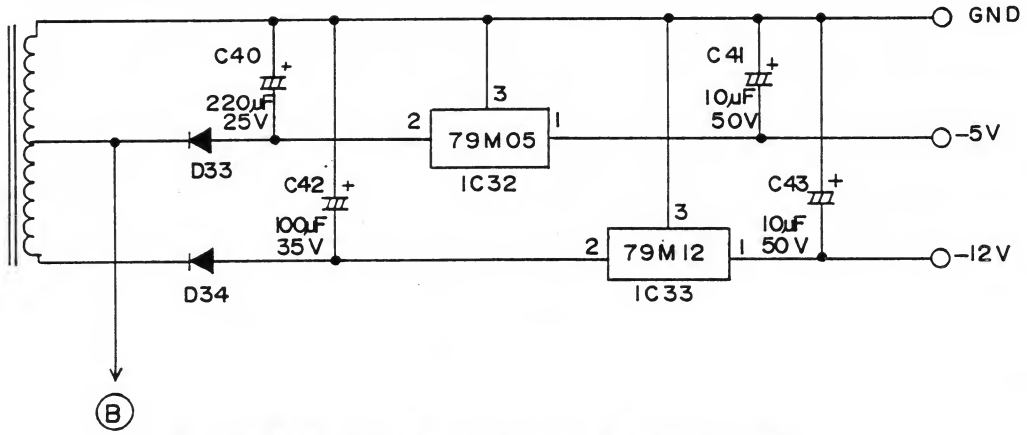


FIGURE 2−8. −5V / −12V SUPPLY CIRCUIT

2.2.2.4 OUTPUT−VOLTAGE STABILIZATION CIRCUIT

The output−voltage stabilization circuit stabilizes the secondary side output voltage by detecting a variation in the +5V voltage and controlling the primary side generation. The reference voltage is detected by the ZD31 cathode. When the voltage is higher than the reference voltage, ZD31 passes current from the cathode to the anode, turns on the PC1 photodiode, and so sends a signal to the primary side. The PC1 phototransistor which receives the signal reduces the time constant of the generation circuit in the switching regulator power IC (IC11) by increasing the collector current. This phototransistor decreases the secondary side output voltage by reducing the switching duty. When the voltage is lower than the reference voltage, the reverse of the above operations is performed. The output voltage is stabilized by these operations being repeatedly performed. Figure 2−9 shows the circuit.

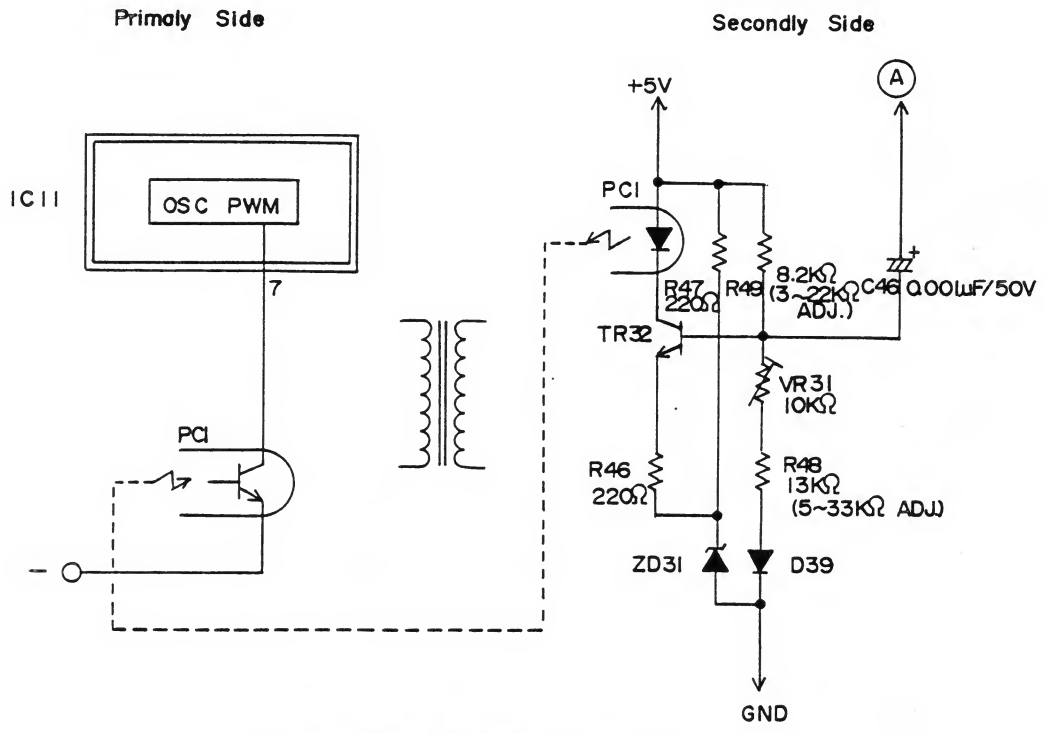


FIGURE 2-9. OUTPUT VOLTAGE STABILIZATION CIRCUIT

2.2.2.5 POWER DOWN CIRCUIT

When the supply voltage drops to the extent that the machine cannot be operated normally, the voltage drop is reported to the main system unit. The POWER DOWN signal is output just before the supply voltage drops due to a power failure or interruption, and sends a top-priority interrupt to the CPU. The voltage detection comparator IC34 (3761) indirectly monitors the input voltage making use of the fact that the output from the +5V transformer is proportional to the primary side input voltage. This comparator also monitors the output voltage of the +5V line. When a drop in one of the voltages is detected, IC34 turns TR33 on and forces the POWER DOWN signal low. Figure 2-10 shows the POWER DOWN circuit.

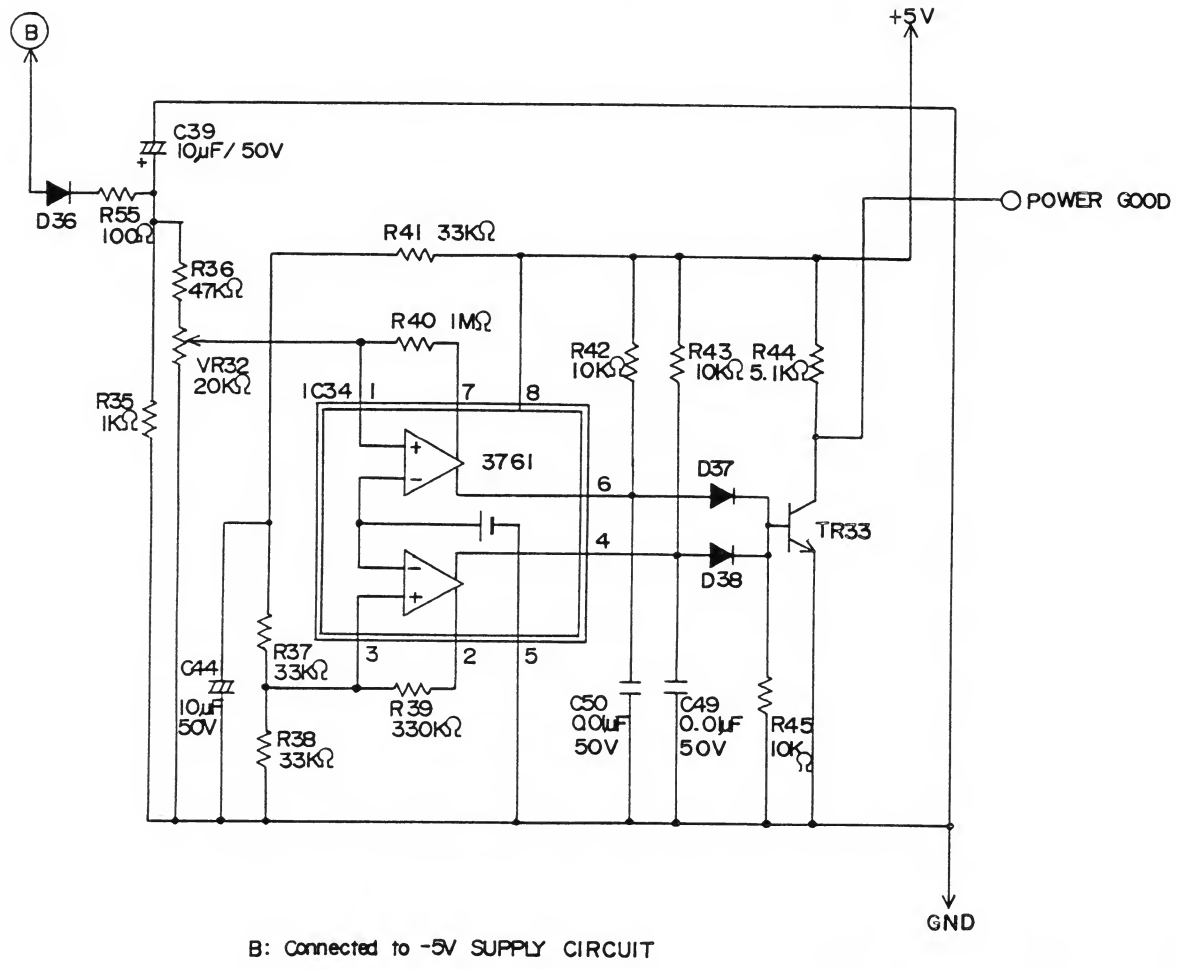


FIGURE 2 – 10. POWER DOWN SIGNAL GENERATION CIRCUIT

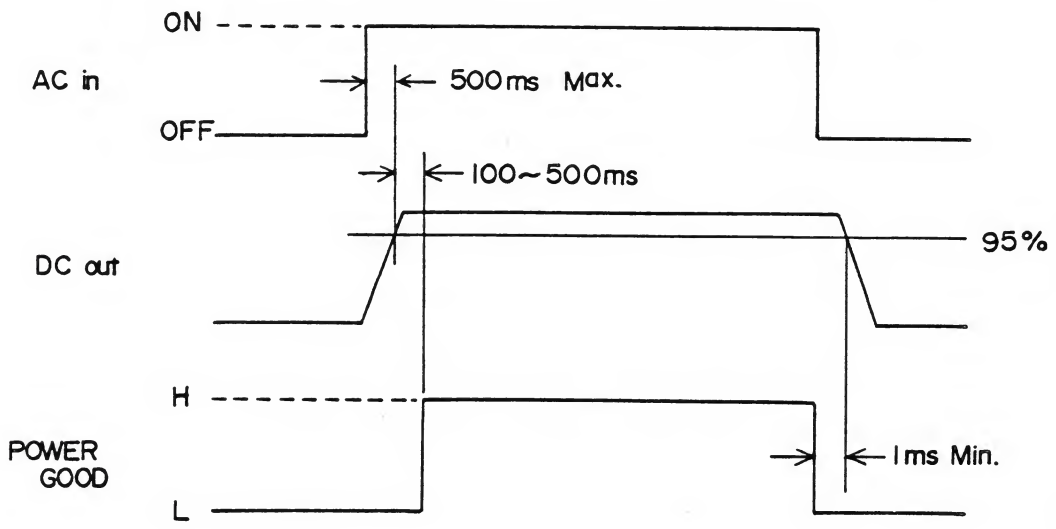


FIGURE 2 – 11. POWER DOWN TIMING CHART

2.3 ANDRO Board Main Control Operations

This section describes the important internal circuits of the EQUITY II+ / EPSON PC AX2 system board. The diagram on the next page shows the relative positions of the custom gate array chips on the system board (ANDRO) and the memory board (ADR-RM3 / ADR-RM3S).

The table below shows the memory map for the EQUITY II+ / EPSON PC AX2 computer system.

TABLE 2-2. MEMORY MAP

ADDRESS	*NAME*	*FUNCTION*
000000 to 09FFFF	640 KB system memory	System memory
0A0000 to 0BFFFF	128 KB video RAM	Reserved for graphics display buffer
0C0000 to 0DFFFF	128 KB I/O Expansion ROM	Reserved for ROM on I/O adapters
0E0000 to 0EFFFF	64 KB reserved	Duplicated code assignment at address FE0000
0F0000 to 0FFFFF	64 KB system board ROM	Duplicated code assignment at address FF0000
100000 to FDFFFF	Extended/Expansion RAM	I/O channel RAM - memory expansion option
FE0000 to FEFFFF	64 KB reserved	Duplicated code assignment at address 0E0000
FF0000 to FFFFFF	64 KB system board ROM	Duplicated code assignment at address 0F0000

2.3.1 SYSTEM CLOCK GENERATION CIRCUIT

All clock signals are supplied by gate arrays GAATCK and GAATCX except the real-time clock (RTC) clock signal. GAATCK and GAATCX generate the following clock signals.

1) System clock (16MHz, 20MHz)
2) NPX clock (8MHz)
3) DMA clock (4MHz, 5MHz)
4) Timer/counter clock (1.19MHz)
5) Keyboard controller clock (6MHz)
6) OSC clock (for expansion slots: 14.31818MHz)
7) SCLK signal (System clock for expansion slots: 8MHz, 10MHz)

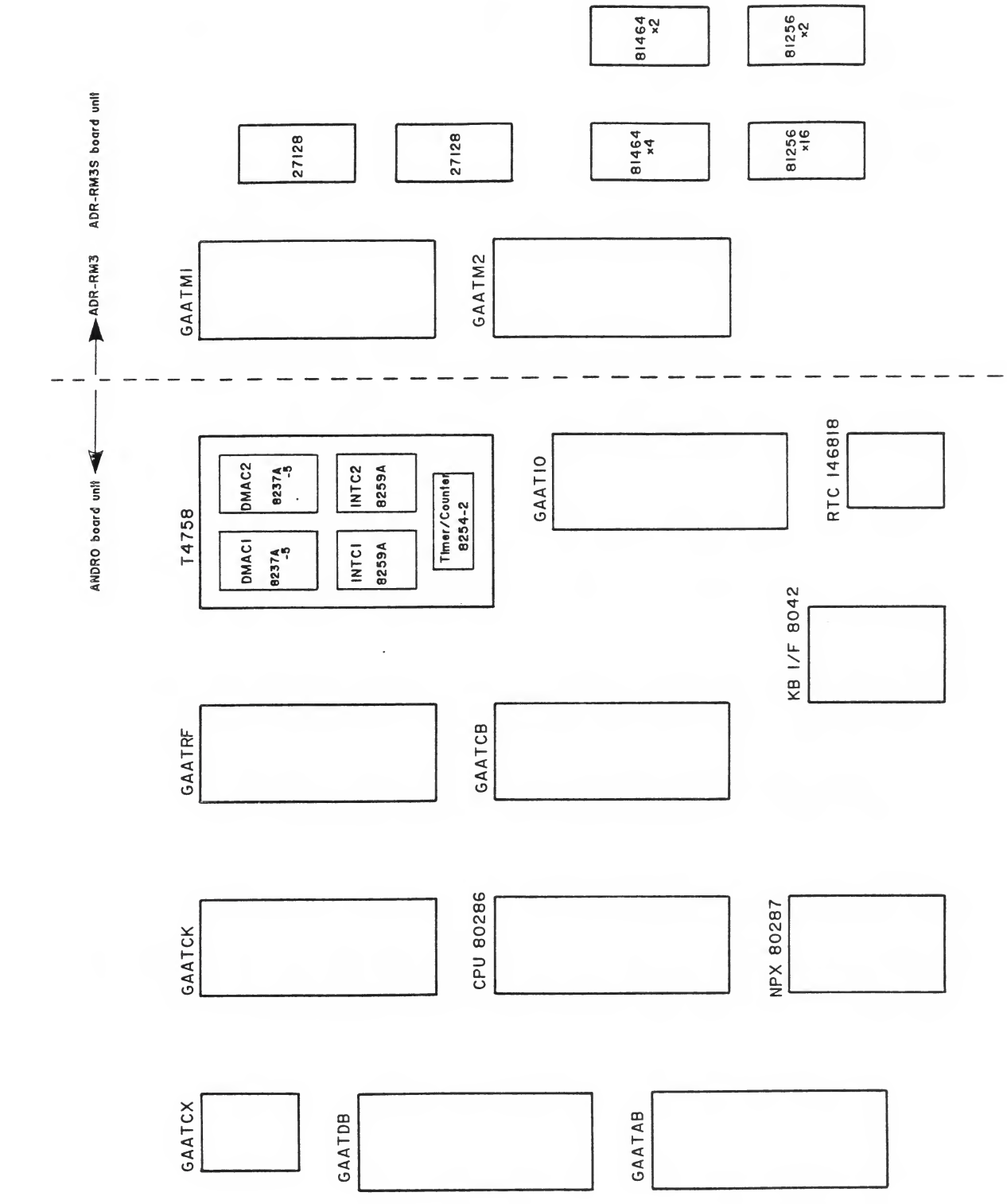


FIGURE 2 – 12. INTERNAL CIRCUIT CONFIGURATION

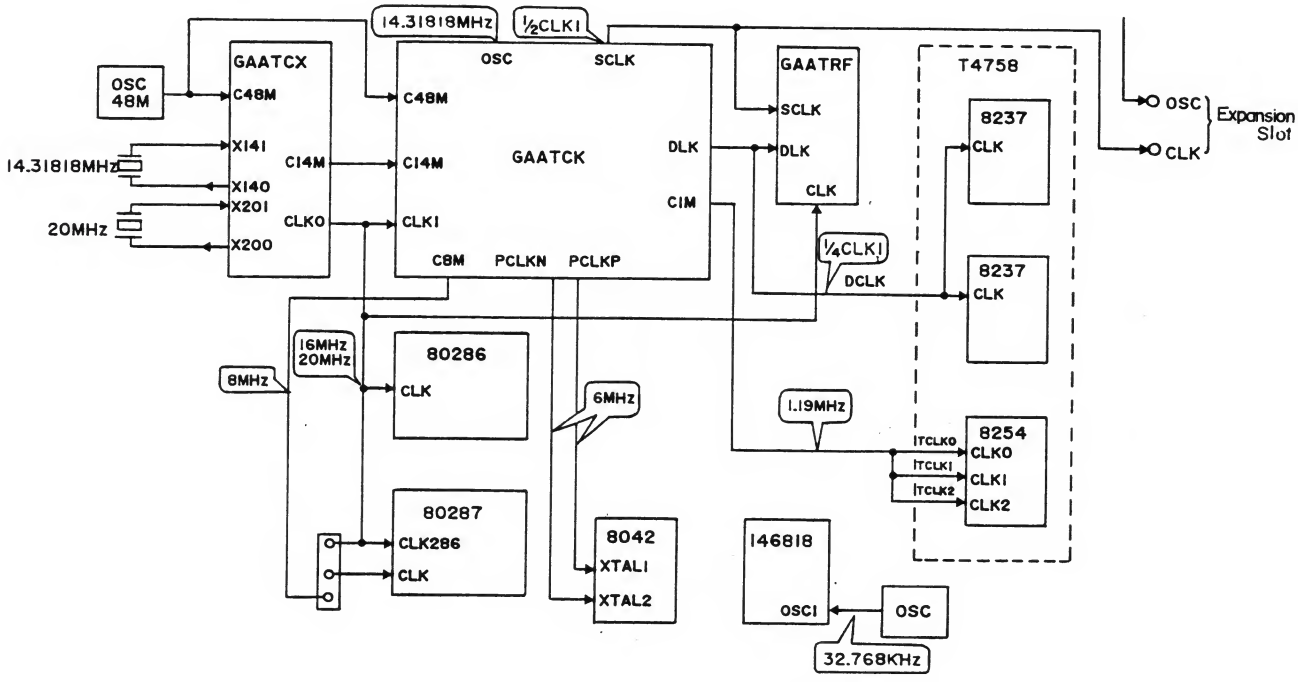


FIGURE 2 – 13. SYSTEM CLOCK GENERATION CIRCUIT

NOTE:Please note the difference between the terms system clock *and* CPU clock. *The 80286 (CPU) divides the system clock by two to obtain its operating clock signal. This manual defines these words as follows:*

System Clock: *Internal "crystal" system clock (20MHz or 16MHz)*
CPU Clock: *The operation speed of the CPU (System Clock/2)*

2.3.1.1 CLOCK SPEED SELECTION

The EQUITY II+ / EPSON PC AX2 has two hardware – selectable CPU clock speeds: 8MHz and 10MHz. CPU clock speed is selected by the position of the slide switch (SW2) on the front panel of the main unit. The gate array GAATCX provides clock speed selection circuitry.

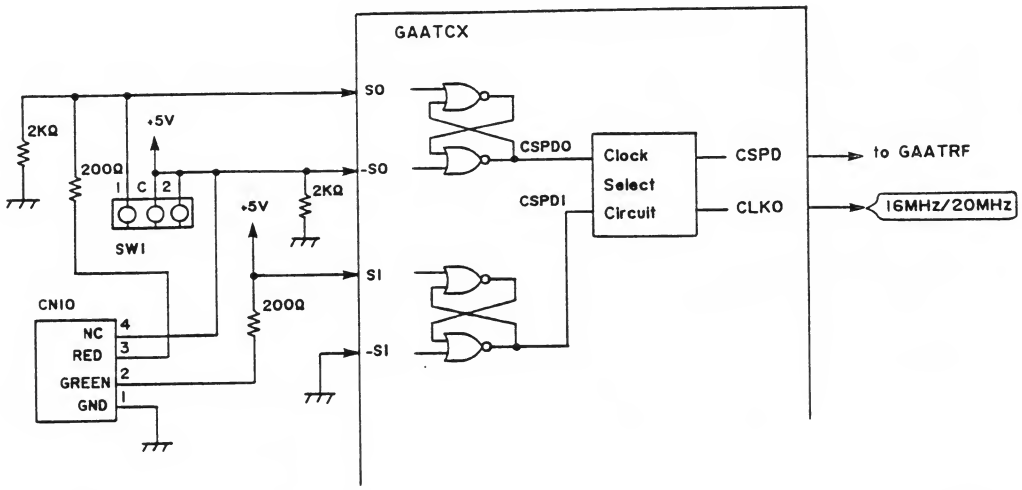


FIGURE 2-14. CLOCK SPEED SELECTION

2.3.1.2 LED INDICATORS

The power-on LED indicator on the front panel is connected to the clock speed change circuitry. Its color indicates the current CPU clock speed as shown below:

TABLE 2-3. LED INDICATIONS

LED INDICATION	*CPU OPERATION SPEED*
ORANGE	8MHz
GREEN	10MHz

2.3.1.3 NPX (80287) CLOCK SPEED SELECTION

The EQUITY II+/ EPSON PC AX2 has two NPX operation speed modes. The first mode, selected by setting system board jumpers J4 and J5 to "A", sets the NPX clock speed to 8MHz regardless of the CPU clock speed. The second mode, selected by setting jumpers J4 and J5 to "B", sets the NPX clock speed to be 2/3 of the CPU clock speed. The table below shows the resulting NPX clock speeds for each mode.

TABLE 2-4. NPX OPERATION SPEED

MODE	*CPU CLOCK*	*NPX CLOCK*
8MHz Mode:	8MHz	8MHz
(J4 and J5 set to "A")	10MHz	8MHz
2/3 CPU Mode:	8MHz	5.33MHz
(J4 and J5 set to "B")	10MHz	6.66MHz

2.3.1.4 OSCILLATORS

There are three oscillators on the ANDRO board: 48MHz, 20MHz and 14.31818MHz. The gate arrays GAATCX and GAATCK receive the timing signals from these oscillators and generate the timing signals shown in the table below.

TABLE 2-5. OSCILLATOR CLOCK SIGNAL FLOW

OSC Clock Signal	*GAATCX Conversion*	*GAATCX Generates*	*GAATCK Conversion*	*GAATCK Generates*	*Connected To*
48MHz	1/3	16MHz	–	–	CPU
	1/3	16MHz	1/2	8MHz	Expansion Slots
	1/3	16MHz	1/4	4MHz	DMA Controller
	–	–	1/6	8MHz	NPX
	–	–	1/8	6MHz	Keyboard Controller
20MHz	1/1	20MHz	–	–	CPU
	1/1	20MHz	1/2	10MHz	Expansion Slots
	1/1	20MHz	1/4	5MHz	DMA Controller
14.31818MHz	1/1	14.31818MHz	1/1	14.31818	Expansion Slots
	1/1	14.31818MHz	1/12	1.19MHz	Timer/Counter

2.3.2 SYSTEM RESET SIGNAL GENERATION

There are three reset signals used in the EQUITY II+ / EPSON PC AX2 computer system.

1) CPU Reset Signal
2) Internal Circuit Reset Signal
3) Expansion Slot Reset Signal

The gate array GAATCK generates these signals under the following conditions:

TABLE 2-6. RESET SIGNAL GENERATION METHODS

RESET SIGNAL	*CAUSE*
CPU Reset Signal	PWGD signal goes low. Reset switch is pushed. RC signal goes active. (Software reset) Shut down cycle is executed.
Internal Circuit Reset Signal	Reset switch is pushed.
Expansion Slot Reset Signal	Reset switch is pushed.

NOTE: The Software Reset command (RC goes active) resets only the CPU. When gate array GAATCK receives the RC signal, it generates the RSCPU signal.

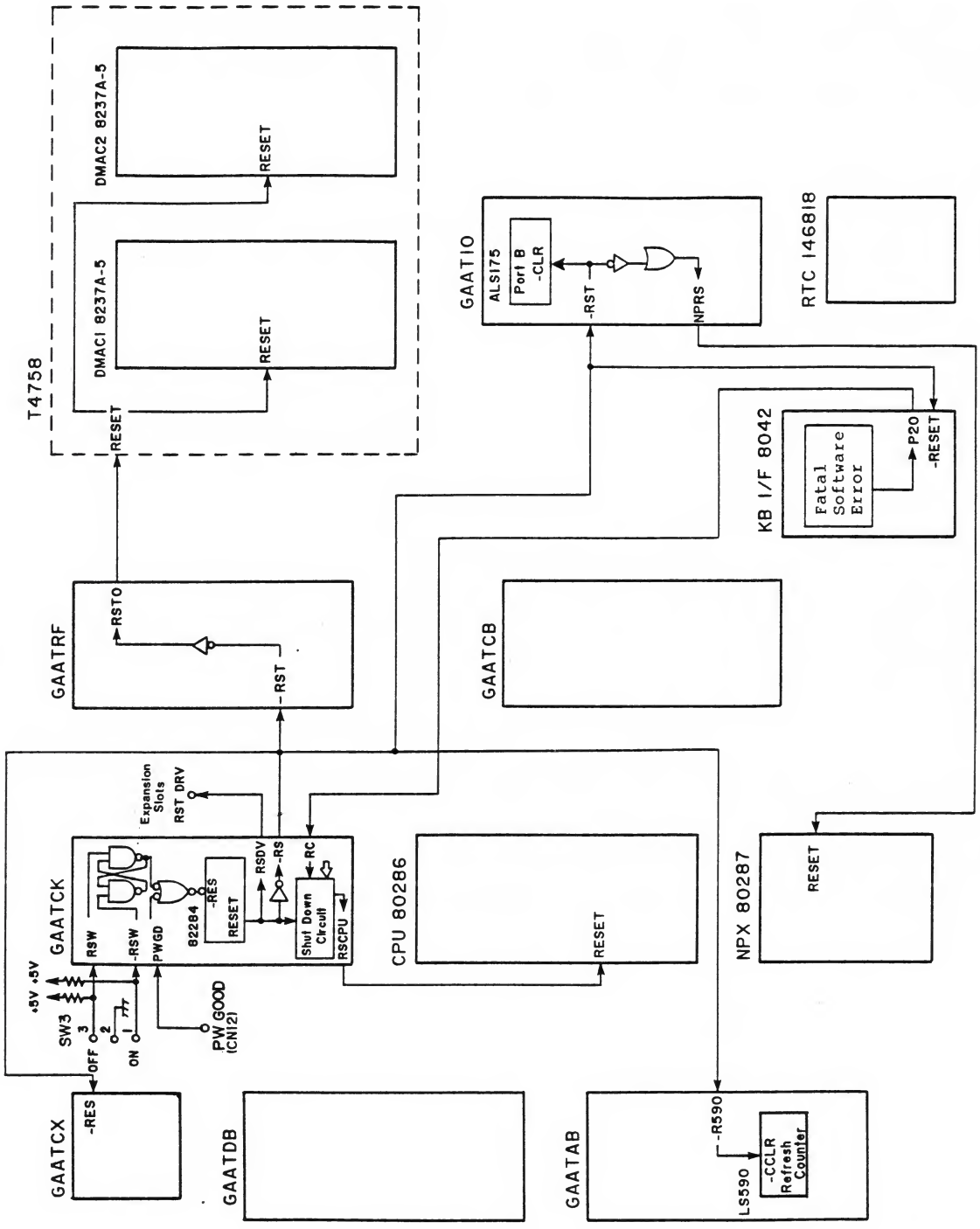


FIGURE 2 – 15. SYSTEM RESET SIGNAL CIRCUIT

2.3.2.1 SYSTEM RESET CIRCUITS

PWGD signal

The power supply unit (ADRPS unit) generates the PWGD (power good) signal. Normally, this signal remains high. If the power supply is unable to supply current within the specified limits, the power supply unit will drive the PWGD signal LOW. A LOW PWGD signal will, in turn, cause GAATCK to activate all three system reset signals (–RS, RSDV, and RSCPU).

Reset switch (SW3)

When the reset switch SW3 is pushed, the GAATCK drives the three system reset signals (–RS, RSDV, and RSCPU) active.

RC signal

The RC signal can be sent, under software control, to GAATCK from P20 pin of the keyboard controller (8042). An active RC signal will cause GAATCK to reset the CPU by generating an RSCPU signal.

Shut down cycle

The Shutdown cycle is one of the 80286's execution cycles. The CPU executes this cycle when it detects a fatal software error and cannot continue the current operation. The CPU indicates this cycle through a combination of the –S0, –S1, and M/–IO signals. If GAATCK detects the CPU Shutdown cycle it generates an active RSCPU signal and resets the CPU.

2.3.3 INTERNAL MEMORY CONTROL CIRCUIT

All system memory chips are located on the ADR–RM3 / ADR–RM3S board. If the system will not boot up it is recommended that the ADR–RM3 / ADR–RM3S board should be replaced first in order to determine whether the problem is caused by faulty RAM chips, or by a fault in another circuit.

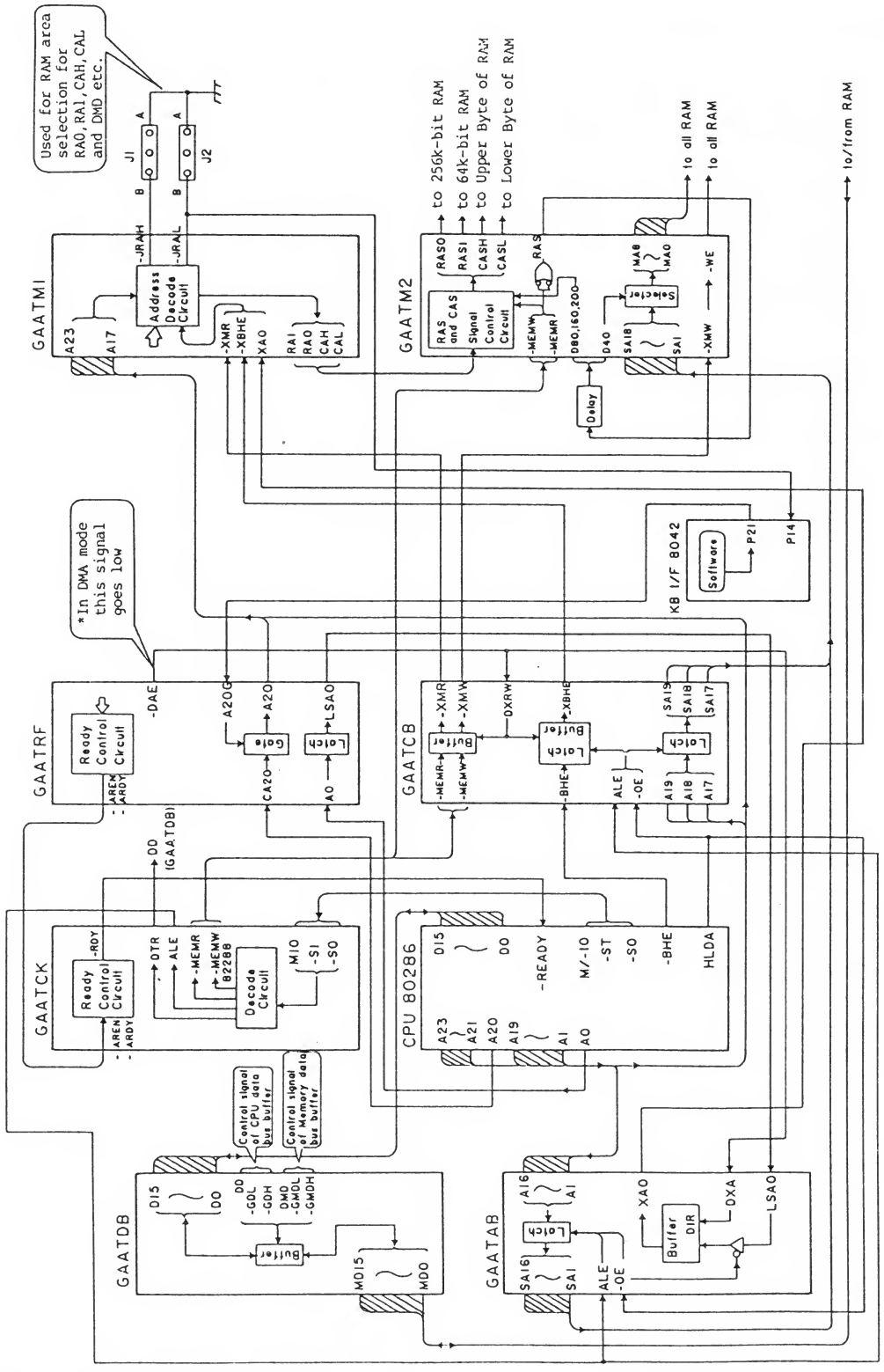


FIGURE 2 – 16. INTERNAL MEMORY CONTROL CIRCUIT

2.3.3.1 RAM CHIP TYPE

There are two kinds of RAM chips on the ADR-RM3 / ADR-RM3S board.

TABLE 2-7. FUNCTION OF RAM CHIPS

RAM CHIP TYPE	*Q'TY*	*FUNCTION*
256K-word by 1bit	16	System memory (512KB)
64K-word by 4bit	4	System memory (128KB)
256K-word by 1bit	2	Parity check
64K-word by 1bit	2	Parity check

2.3.3.2. RAM CHIP ADDRESSES

The system memory RAM chips are located in the following addresses.

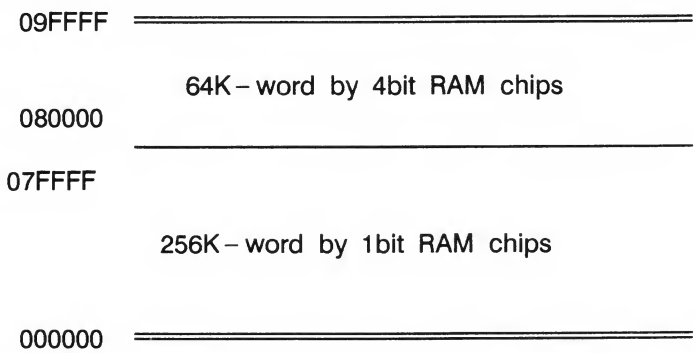


FIGURE 2-17. RAM CHIP ADDRESSES OF SYSTEM MEMORY

2.3.3.3 SYSTEM MEMORY JUMPERS

It is possible to disable some of the system memory by setting jumper connectors J1 and J2 on the ADR-RM3 / ADR-RM3S board.

TABLE 2-8. JUMPER CONNECTOR FUNCTION

Jumper		
J2	*J1*	*Functional Description*
A	*A*	*640K Bytes of RAM Enabled: 09FFFF - 000000*
A	*B*	*512K Bytes of RAM Enabled: 07FFFF - 000000*
B	*A*	*(Not used)*
B	*B*	*256K Bytes of RAM Enabled: 03FFFF - 000000*

2.3.3.4 MEMORY CONTROL CIRCUIT OPERATION

Address signals

The address signal (on address bus lines A0 to A23) is generated by the CPU. GAATM2 (Memory control gate array 2) receives address signals A1 to A18 for the RAM chip address signals. GAATM1 (Memory control gate array 1) receives signals A0 and A17 – A23 and then generates the RAS, CAS and other memory address selection signals.

GAATRF, in combination with the 8042, controls the A20 signal from the CPU to insure correct performance of the A20 signal throughout the bus. Circuitry in the 8042 and GAATRF insure that the value of A20 will be 0 when the CPU is in REAL mode. Refer to section 2.3.14.6 for a logic table regarding A20 control.

The SA0 signal from gate array GAATAB is used during RAM refresh cycles, but is not used by the memory control circuit during RAM reads or writes.

Data bus signals

Gate array GAATDB controls the memory data bus through its internal data bus buffer.

Read/Write control signals

The CPU bus cycle – type outputs – S0, – S1, and M/ – IO, are received by gate array GAATCK. GAATCK, in turn, generates – MEMR and – MEMW signals which are used by GAATM2 to generate RAS and CAS signals. During a Write cycle GAATM2 receives the – XMW (– MEMW) signal from GAATCB, and generates the WE (Write Enable) signal for the RAM chips. During a Read cycle GAATM1 receives the – XMR (– MEMR) signal from GAATCB, and generates the RAS and CAS signals.

DRAM refresh control circuit

The DRAM Refresh circuitry is discussed in detail in section 2.3.11.

2.3.4 BYTE/WORD ACCESS & 16 – 8 BIT DATA CONVERSION

16 – 8 bit data conversion occurs during word transmission to an even address of an 8 bit device.

TABLE 2-9. CPU DATA ACCESS MODE DIAGRAM LIST

MODE	*DATA TRANSMISSION TO*	*REFERENCE*
Byte transmission of EVEN address	16-bit device	Figure 2-9
Byte transmission of ODD address	16-bit device	Figure 2-20
Word transmission of EVEN address	16-bit device	Figure 2-21
Word transmission of ODD address	16-bit device	- - -
Byte transmission of EVEN address	8-bit device	Figure 2-22
Byte transmission of ODD address (read)	8-bit device	Figure 2-23/2-24
Byte transmission of ODD address(write)	8-bit device	Figure 2-25
Word transmission of EVEN address	8-bit device	Figure 2-26

2.3.4.1 DATA BUS CONTROL SIGNAL ON GAATDB

The gate array GAATDB includes five 8-bit buffers. These buffers use gate control and direction signals generated by other gate arrays. The following table describes gate control signals and direction signals.

TABLE 2-10. FUNCTIONS OF CONTROL SIGNAL ON GAATDB.

NAME	*DESCRIPTION*
D245, G245	Controls Data Bus Conversion (High byte - - > low byte) (Low byte - - > High byte)
DMD, -GMDH, -GMDL	Controls Memory Data Bus (Disabling, Direction control)
DD, -GDH, -GDL	Controls CPU Data Bus (Disabling, Direction control)
CBA, SBA	Controls Data Bus Latching (During 16-8 bit data conversion)

2.3.4.2 WORD TRANSMISSION TO ODD ADDRESSES

Transmission of a data Word to an odd address (on either a 16-bit or 8-bit device) is treated as a series of two one-byte transmissions. The CPU transmits the first byte of the word to the odd address, then transmits the second byte of the word to the following even address. The circuitry to perform this conversion is shown in Figures 2-3-8 and 2-3-7 for 16-bit devices, and Figures 2-3-11/12 (R/W) and 2-3-10 for 8-bit devices.

The instruction set for the 80286 CPU provides the capability to perform this function automatically, and if the programmer anticipates Word transmissions to odd addresses the application may be coded to do so directly.

COFF signal

COFF is generated by GAATRF and is used by GAATCK to generate the two 8-bit device read/write signals during word access to odd addresses. GAATDB also receives this signal and uses it to latch low-byte data in its internal LS646 buffer. When GAATCK receives an active COFF signal, the read/write signal of GAATCK goes inactive.

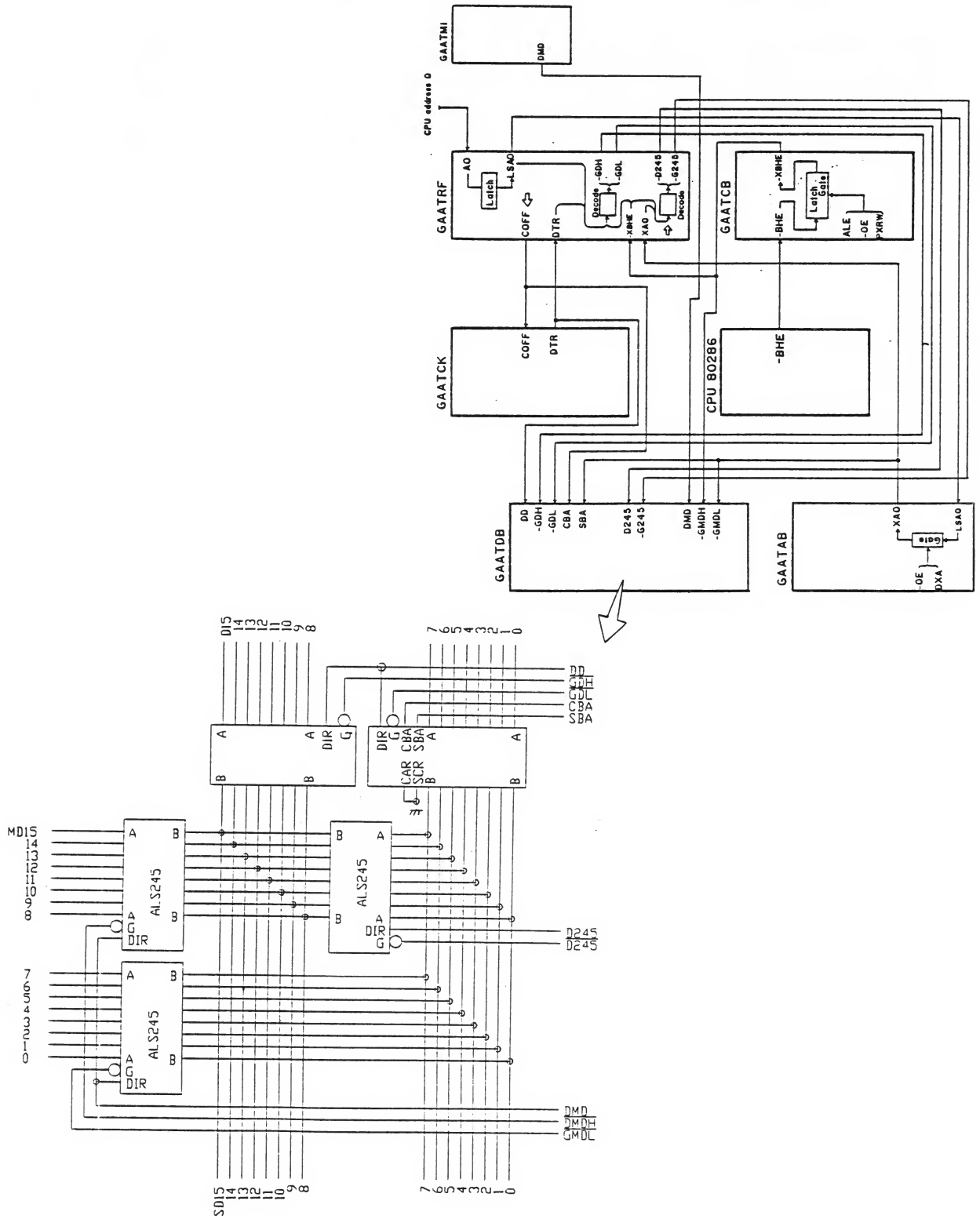


FIGURE 2 – 18. BYTE/WORD ACCESS & 16 – 8 BIT DATA CONVERSION

LSA0 and XA0 signals

LSA0 is generated by GAATRF. During a 16 – 8 bit data conversion GAATRF does not use the CPU A0 signal to generate the LSA0 signal. (The internal circuit of GAATRF generates the LSA0 signal from the CPU A0 signal when not in conversion mode. The internal buffer LS646 of the GAATDB inputs this signal (XA0) to send the latched data to the CPU. 8 – bit devices also receive this signal for address determination. During word – to – byte conversions this signal is changed from 0 to 1 by GAATRF.

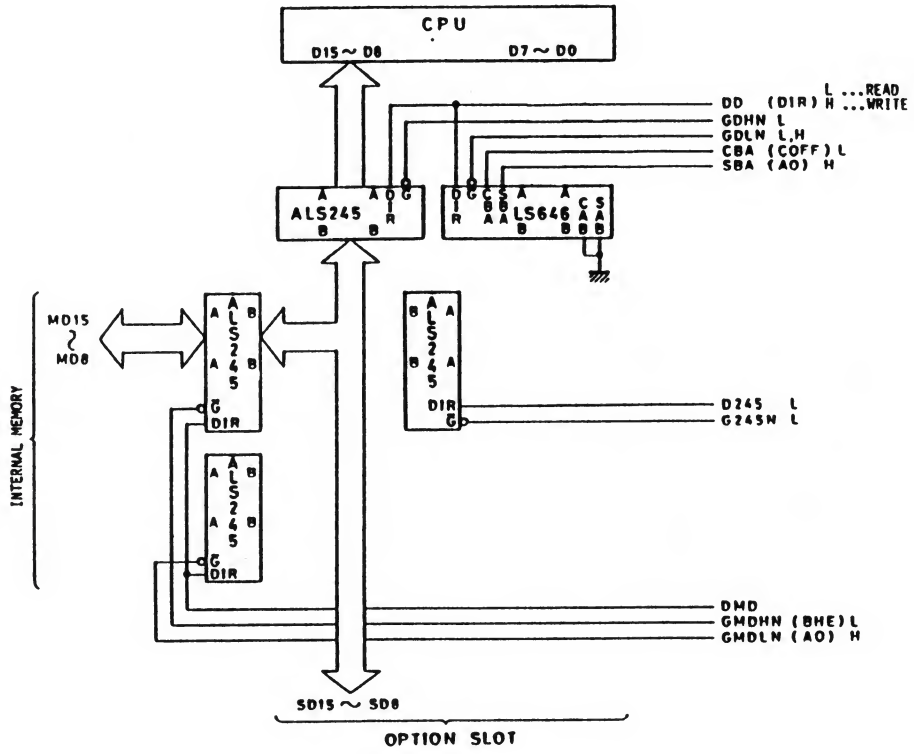


FIGURE 2 – 19. DATA TRANSMISSION TO 16 BIT DEVICE (BYTE TRANSMISSION OF EVEN ADDRESS)

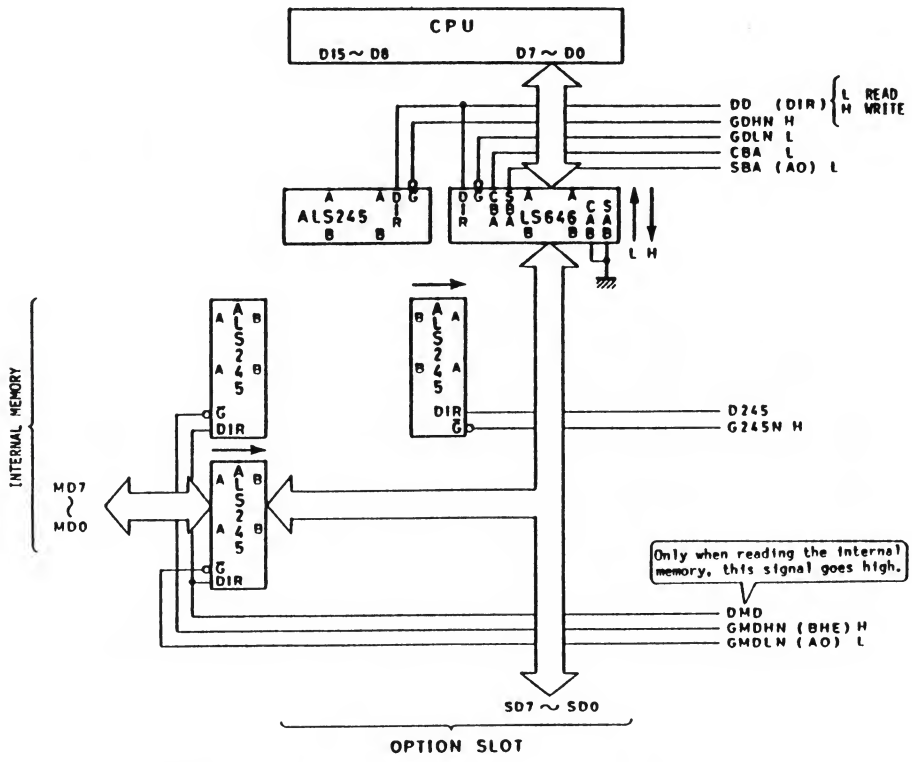


FIGURE 2 – 20. DATA TRANSMISSION TO 8 BIT DEVICE (BYTE TRANSMISSION OF EVEN ADDRESS)

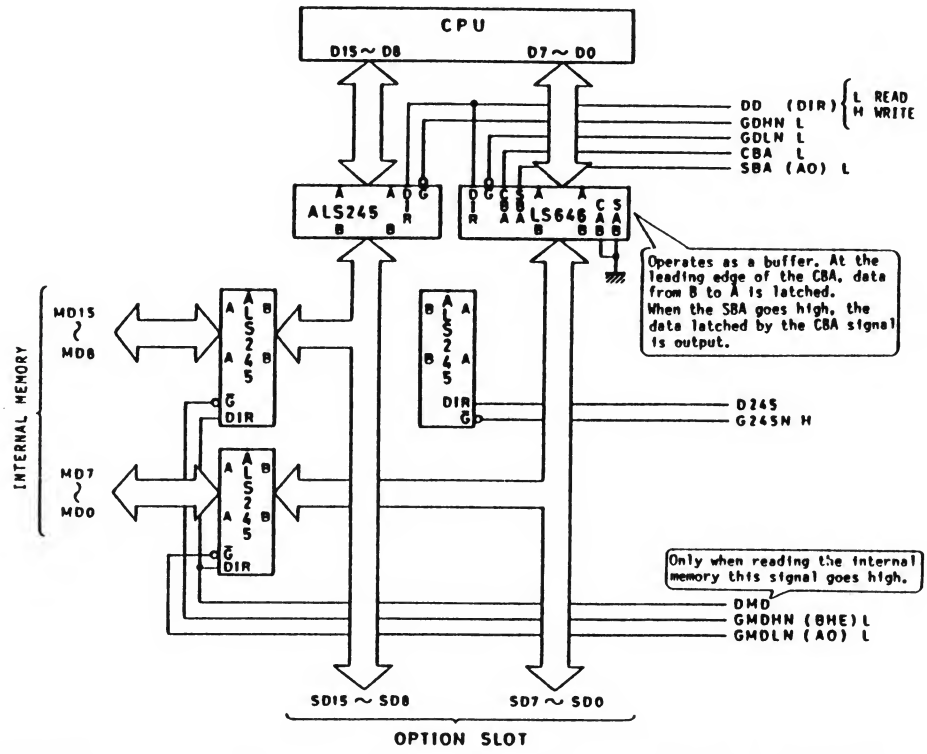


FIGURE 2-21. DATA TRANSMISSION TO 8 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS)

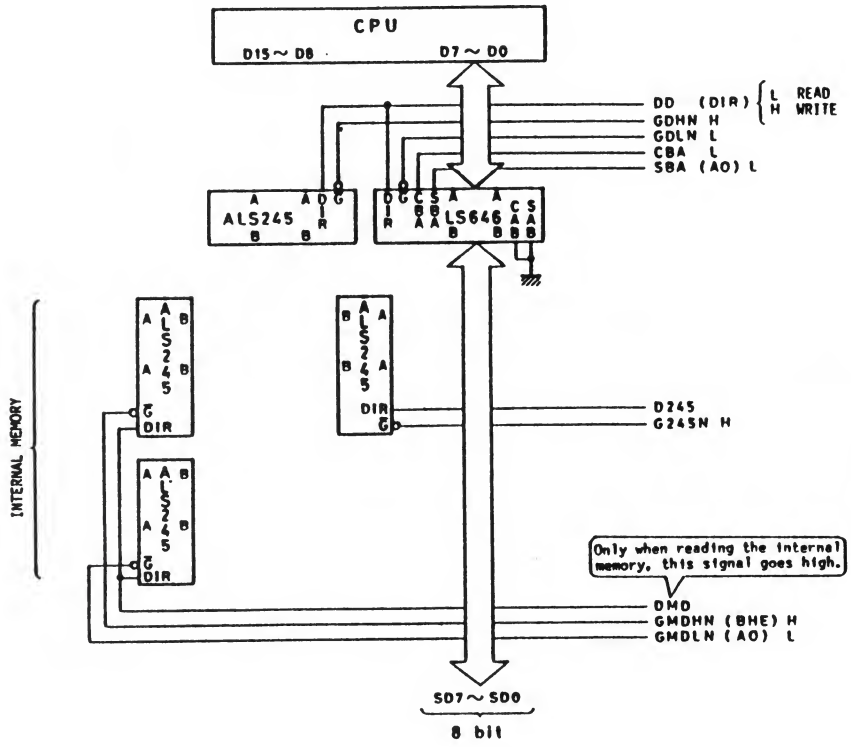


FIGURE 2 – 22. DATA TRANSMISSION TO 8 BIT DEVICE (BYTE TRANSMISSION OF EVEN ADDRESS)

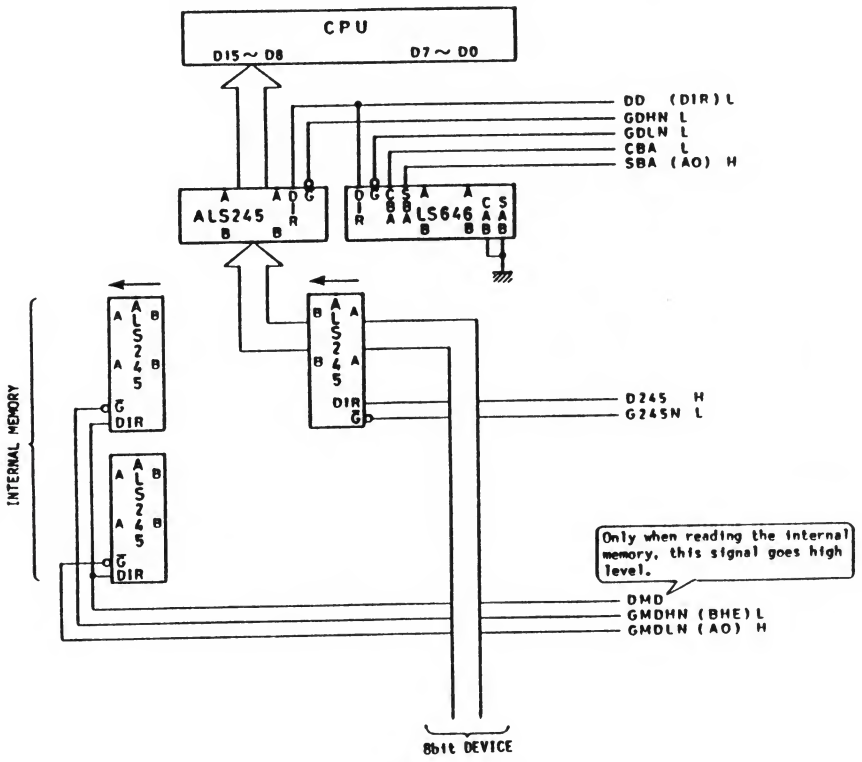


FIGURE 2-23. DATA TRANSMISSSION TO 8 BIT DEVICE (BYTE TRANSMISSION OF ODD ADDRESS, READ MODE)

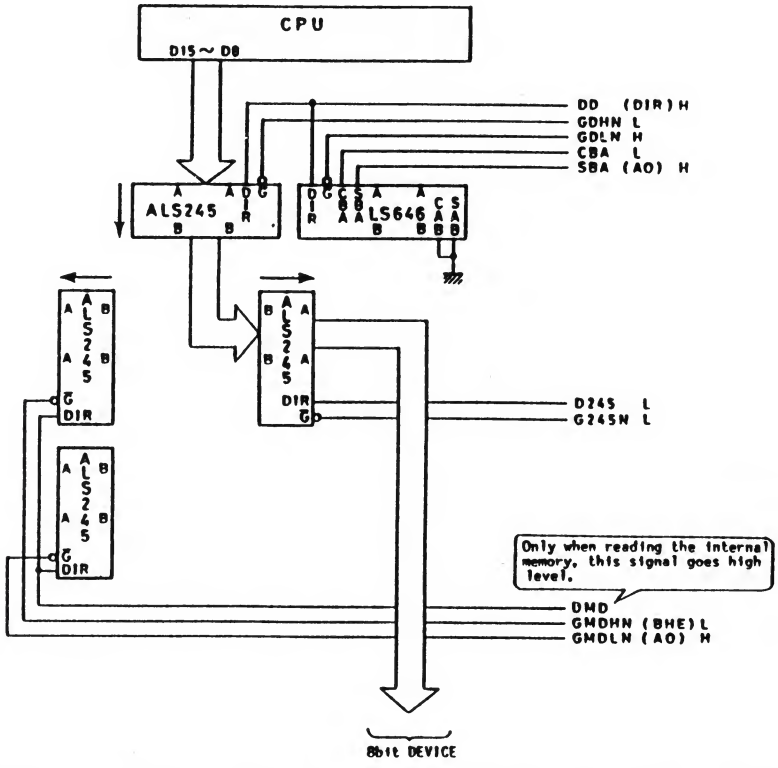


FIGURE 2-24. DATA TRANSMISSION TO 8 BIT DEVICE (BYTE TRANSMISSION OF ODD ADDRESS, WRITE MODE)

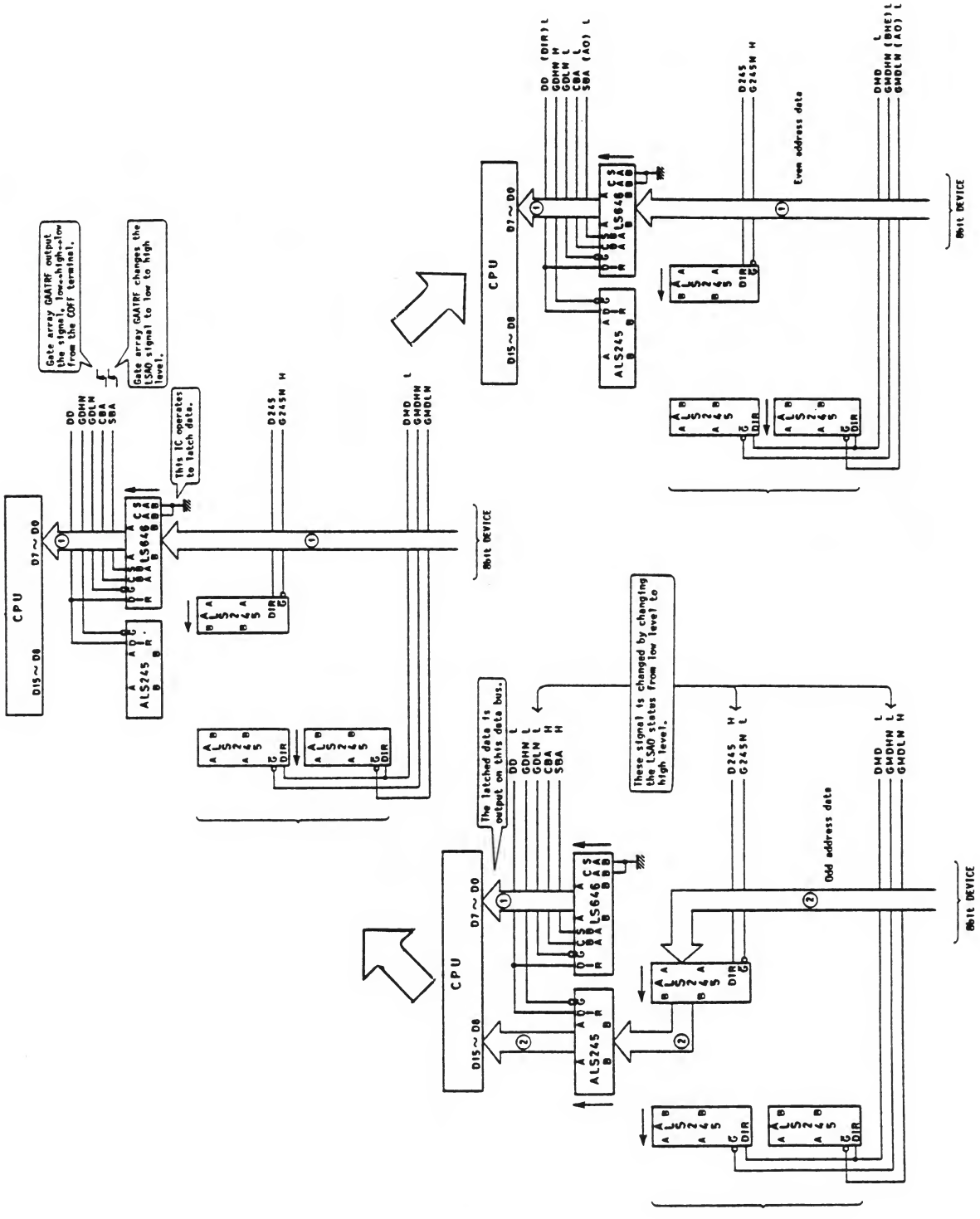
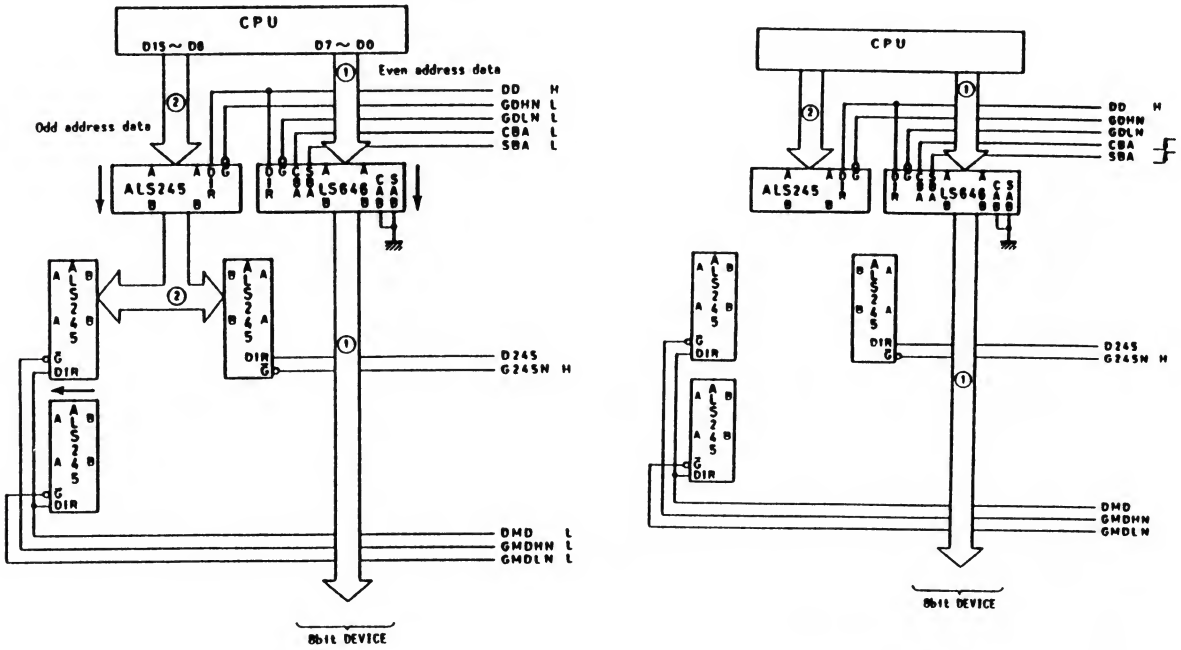


FIGURE 2 – 25. DATA TRANSMISSION TO 8 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS, READ MODE) 16 – 8 BIT DATA CONVERSION

* The 8 bit device reads Data 1.



* The 8 bit device reads Data 2.

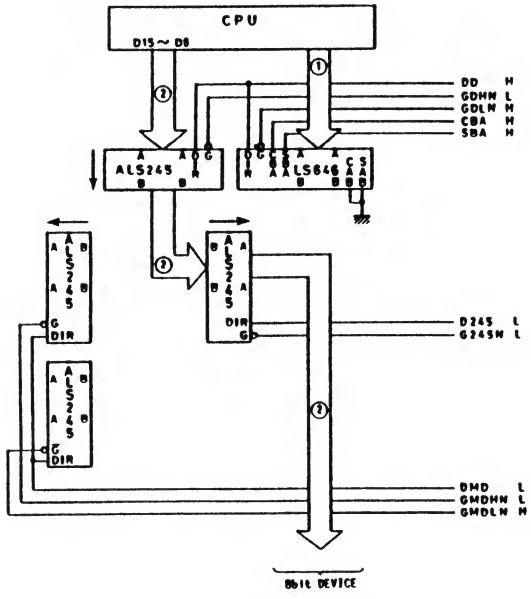


FIGURE 2-26. DATA TRANSMISSION TO 8 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS, WRITE MODE) 16-8 BIT DATA CONVERSION

2.3.5 I/O DEVICE ACCESS CIRCUIT

The GAATIO generates the I/O device chip select signals by decoding address signals. An ALS245 is used in the data transmission between the CPU and the I/O devices.

2.3.6 DMA CONTROL CIRCUIT

There are two Direct Memory Access controllers (DMACs) on the system board (as part of the T4758). Direct Memory Access allows the transfer of blocks of data between memory and I/O devices. DMA is accomplished on DMA "channels" and controlled by the DMA controllers, bypassing the CPU (and using only half the number of bus cycles required by a CPU-controlled data transfer). Conseqently, during a DMA cycle the CPU gives up control of the bus to the DMA controller until the data transfer is completed.

DMAC-1 is the "master" DMAC and controls 8-bit DMA. DMA-2 is the "slave" DMAC and is used only during 16-bit DMA. A Page Register, included in gate array GAATIO, is also used to output the address "page" signals (address lines A16 to A23) during DMA.

This section describes the following items.

1) Page register circuitry
2) 8-bit DMA (Internal memory -- I/O)
3) 8-bit DMA (Internal memory -- Internal memory)
4) 16-bit DMA (Internal memory -- I/O)

2.3.6.1 PAGE REGISTER CIRCUITRY

GAATIO includes a page register. The function of the page register is identical to an LS612. Table 2-11 describes its function.

TABLE 2-11. EXPLANATION OF 74LS612

GAATIO PIN	*74LS612*		*GAATIO PIN*
XD7	D7	MD7	A23
¦	D6	MD6	¦
¦	D5	MD5	¦
¦	D4	MD4	¦
¦	D3	MD3	¦
¦	D2	MD2	¦
¦	D1	MD1	A17
XD0	D0	MD0	XA16/-AEO1
-XIW	STB		
-XIR	R/W		
-XA0	RS0	MA0	-DACK7 AND -DACK3
¦	RS1	MA1	-DACK2 AND -DACK6
¦	RS2	MA2	-DACK0 NAND -RFH
-XA3	RS3	MA3	-DACK4
(-CS)	CS	ME	-ACK

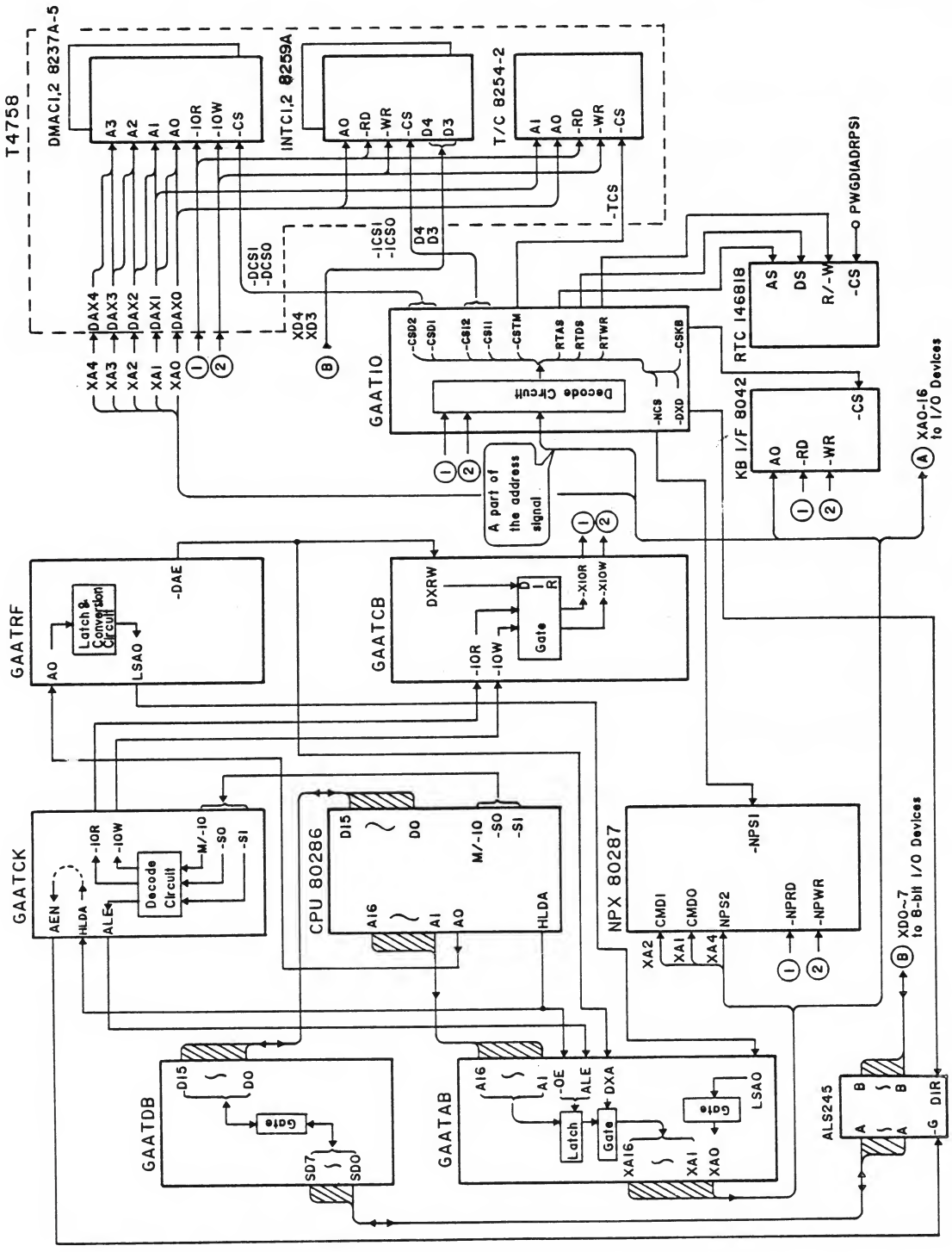


FIGURE 2-27. I/O DEVICE ACCESS CIRCUIT

The Page Register has sixteen 8-bit registers. The R/W signal and the STB signal are used together as a read/write signal. RS0 to RS3 are used as register-select signals when writing data into the Page Register. MA0 to MA3 are the register-select signals used during data output. Likewise, data is sent to the Page Register through D0 to D7. Data is sent from the Page Register on lines MD0 to MD7. When the ME signal is active, data written to the Page Register will also be put on lines MD0 to MD7.

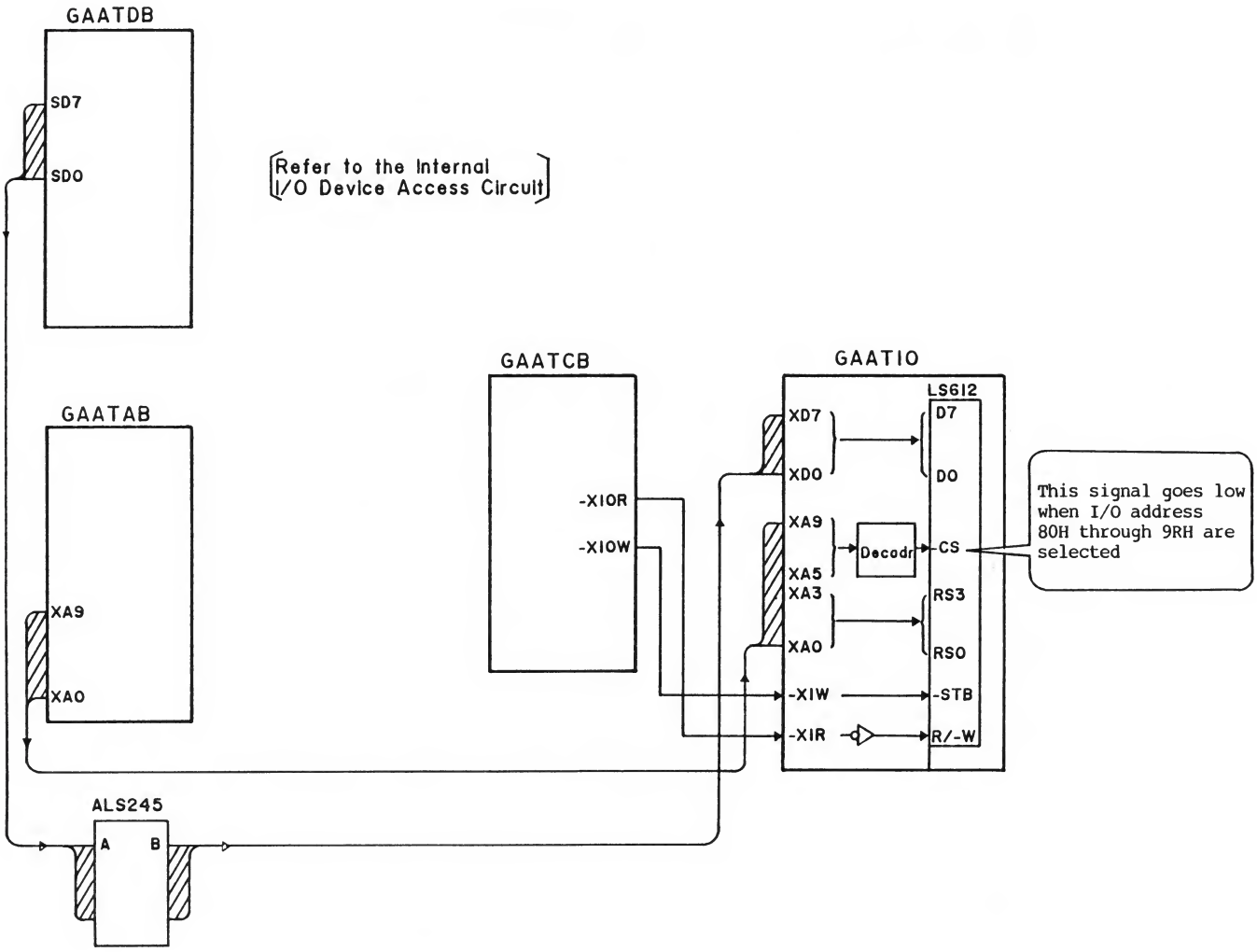


FIGURE 2-28. PAGE REGISTER CIRCUIT

2.3.6.2 8-BIT DMA (INTERNAL MEMORY I/O)

Figure 2-29 shows an 8-bit DMA Memory - I/O operation. During a DMA cycle (when the DMAC has control of the bus) GAATIO lines -MEMR, -MEMW, -IOR and -IOW are output signals. When the CPU has control of the bus, these signals are input signals.

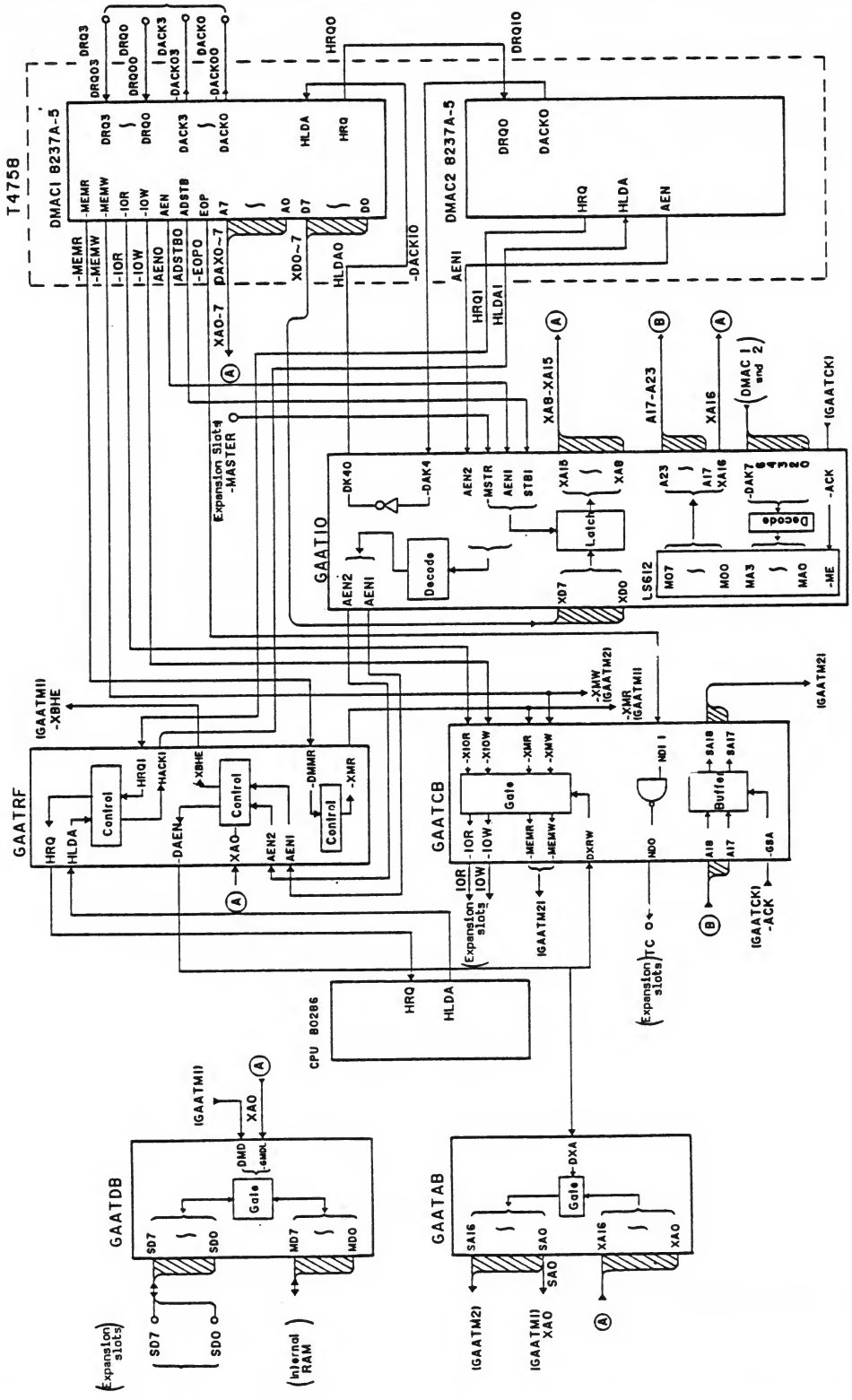


FIGURE 2-29. 8-BIT DMA (INTERNAL MEMORY I/O)

2.3.6.3 8 – BIT DMA (INTERNAL MEMORY – INTERNAL MEMORY)

Figure 2 – 30 shows an 8 – bit DMA Memory – Memory operation. First, the DMA controller stores the memory data. Next, the DMA controller changes the address signal and writes the stored data to the new memory address.

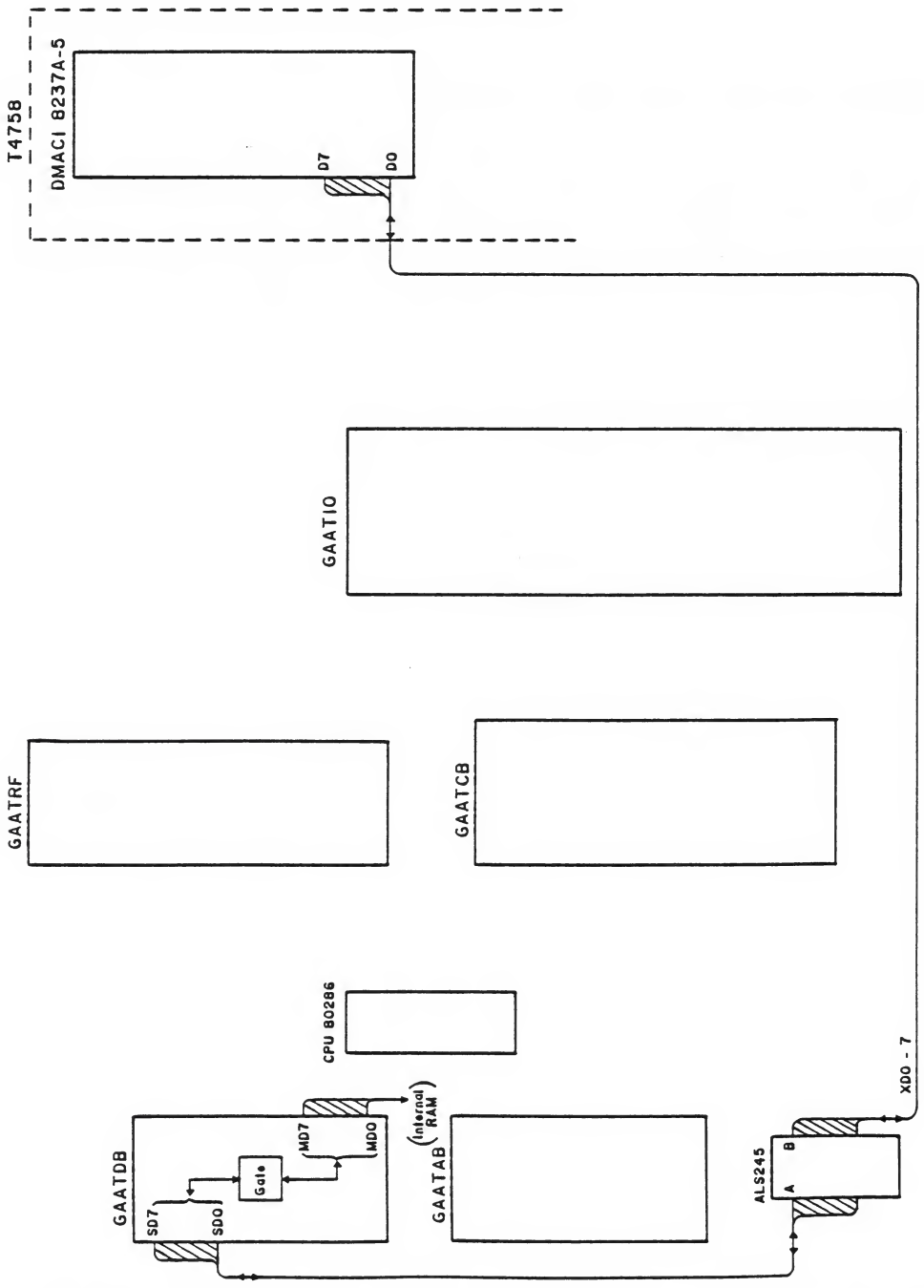


FIGURE 2 – 30. 8 – BIT DMA (INTERNAL MEMORY – INTERNAL MEMORY)

2.3.6.4 16 – BIT DMA (INTERNAL MEMORY – I/O)

DMAC2 controls 16 – bit DMA. In this mode, gate array GAATRF outputs the XA0 and XBHE (Internal Bus High Enable) signals. Both the XA0 and XBHE signals are LOW. DMAC2's A0 signal is not connected to Internal address bus bit 0 (XA0). Instead, the XA0 signal is output from GAATRF.

2.3.7 READY SIGNAL CONTROL CIRCUIT

Gate array GAATRF controls wait state insertion. The wait state is executed to allow adequate timing for internal and external devices. To request wait states, GAATRF sends an – ARDY (Asynchronous – Ready) signal and an – AREN (Asynchronous – Ready Enable) signal. The number of wait states is fixed except for 16 – bit ROM and a 16 – bit expansion bus device access. During 10MHz operation the number of wait states is jumper – selectable for these devices.

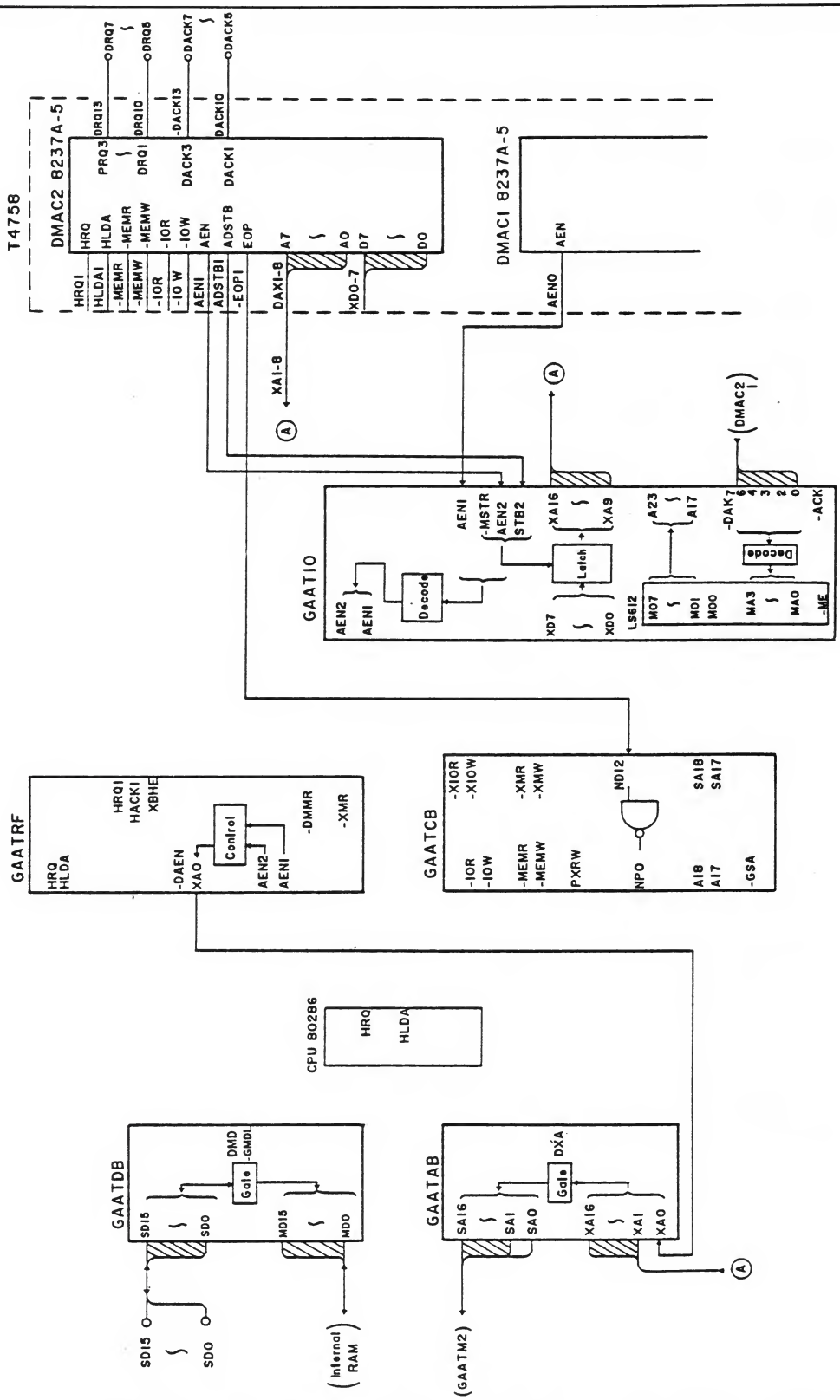


FIGURE 2-31. 16-BIT DMA (INTERNAL MEMORY - I/O)

TABLE 2 – 12. DEVICE ACCESS TIMES AND WAIT CYCLES

DEVICE	Wait Cycles [Total Cycles] Bus Cycle Time 8 MHz	10 MHz
16 – Bit Memory (16 – Bit Bus Operation)		
System DRAM (00000 – 9FFFF)	1 [3] .375µs	1 [3] .3µs
ROM (0E0000 – 0FFFFF FE0000 – FFFFFF)	1 [3] .375µs	1 or 2 [3 or 4] .3µs or .4µs
I/O Channel*	1 [3] .375µs	1, 2, 3, or 4 [3, 4, 5, or 6] .3µs, .4µs, .5µs, or .6µs
8 – Bit Memory On I/O Channel (8 – Bit Bus Operation)	4 [6] .75µs	8 [10] 1.0µs
8 – Bit Memory On I/O Channel (16 – Bit Operation)	10 [12] 1.5µs	18 [20] 2.0µs
16 – Bit I/O On I/O Channel (16 – Bit Bus Operation)	1 [3] .375µs	3 [5] .5µs
8 – Bit I/O On I/O Channel (8 – Bit Bus Operation)	4 [6] .75µs	8 [10] 1.0µs
8 – Bit I/O On I/O Channel (16 – Bit Bus Operation)	10 [12] 1.5µs	18 [20] 2µs

TABLE 2-13. WAIT CYCLE SELECTION

JUMPER J3 J2 J1	*NUMBER OF WAIT CYCLES*
B B	4 Wait Cycles for 16-bit Expansion Bus DRAM
B A	3 Wait Cycles for 16-bit Expansion Bus DRAM
A B	2 Wait Cycles for 16-bit Expansion Bus DRAM
A A	1 Wait Cycle for 16-bit Expansion Bus DRAM
A	1 Wait Cycle for EPROM Access
B	2 Wait Cycles for EPROM Access

2.3.7.1 ADDITIONAL WAIT STATE INSERTION

Additional wait states may be inserted by asserting the expansion bus control signal IOCHRDY (I/O Channel Ready - Expansion bus pin A10). When IOCHRDY is high, a wait cycle will be inserted.

2.3.7.2 ZERO WAIT CYCLE REQUEST

For No Wait State operation the -0WS signal is provided on the expansion bus (pin B8). This signal is low active.

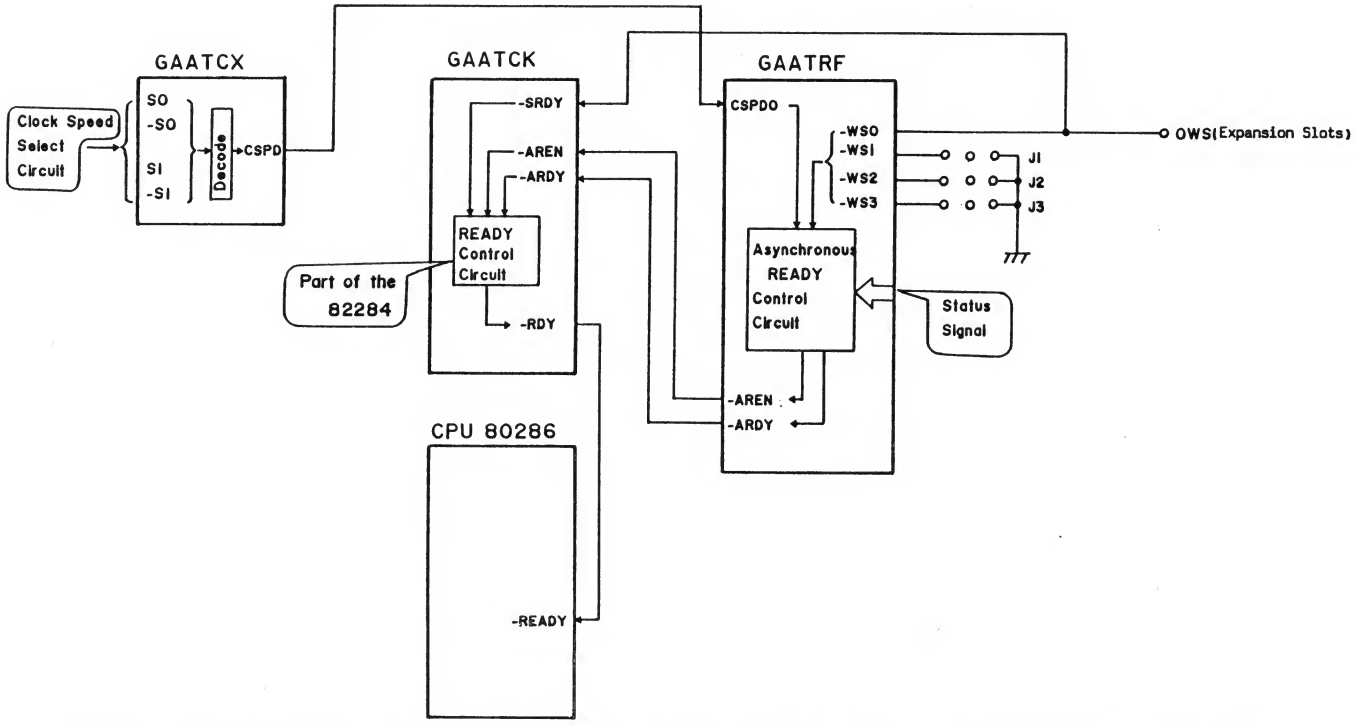


FIGURE 2-32. READY SIGNAL CONTROL CIRCUIT

2.3.8 COMMAND DELAY SIGNAL CONTROL CIRCUIT

Some devices require more than the standard amount of time between the end of one bus cycle and the beginning of the next command cycle. The Command Delay (CDLY) signal control circuit provides adequate timing margins for such devices by delaying the start of the next command cycle (–IOW, –MEMW, –IOR, etc.). The command delay function is executed automatically by GAATRF (and sent to GAATCK) during any I/O access cycle (including Interrupt Acknowledge) or expansion–bus 8–bit memory access. The amount of delay is 0.5 system clocks (SCLK) during 8MHz operation, and 1 SCLK during 10MHz operation.

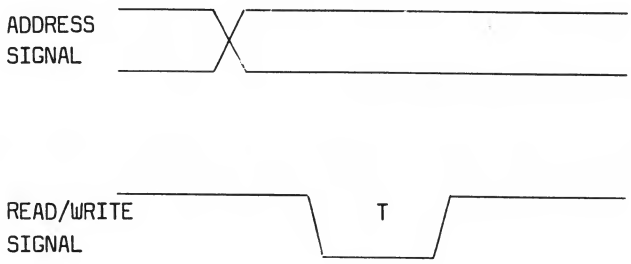


FIGURE 2–33. TIMING BETWEEN ADDRESS SIGNAL AND READ/WRITE SIGNAL

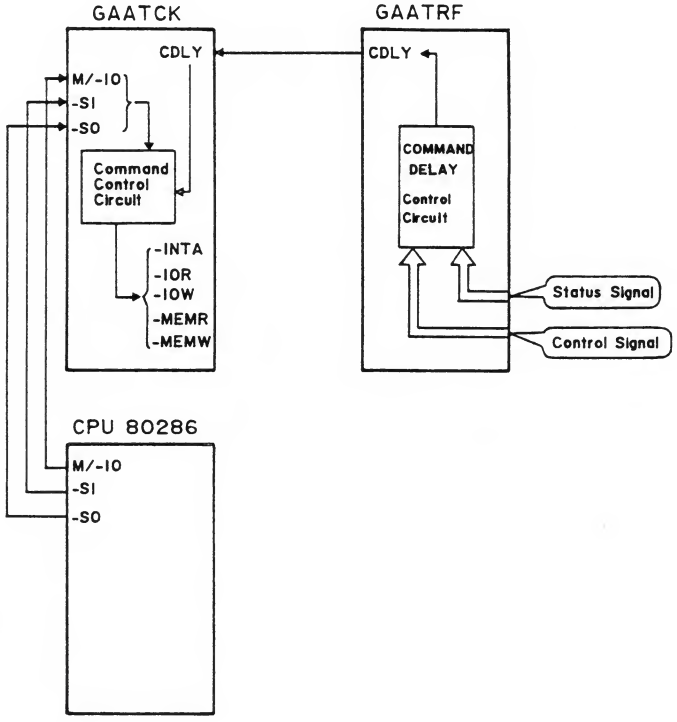


FIGURE 2–34. COMMAND DELAY CONTROL CIRCUIT

2.3.9 INTERRUPT CONTROL CIRCUIT

There are two 8259A – compatible interrupt controller (INTC) circuits on the system board (as part of the T4758), supporting up to 15 interrupt levels. The two INTCs are "cascaded" . Figure 2 – 35 shows interrupt control circuit operation.

2.3.10 ROM ACCESS CIRCUIT

ROM size is selectable by setting jumper J3 on the memory board (ADR – RM3). Setting J3 to "A" selects 128K – bit ROM chips; setting J3 to "B" selects a ROM – chip size of 256K – bits. The recom – mended access time for ROM chips of either type is 150ns.

2.3.11 DRAM REFRESH CIRCUIT

An 8254 – 2 compatible timer/counter is used to control the refresh interval time. The refresh address is sent from an 8 – bit binary counter in gate array GAATAB. During DRAM refresh, the CPU executes a bus hold cycle. The RFNO (Refresh output) signal is important. From this signal gate array GAATM1 generates the RA0 and RA1 signals (RAS signal), and GAATM2 generates the refresh address. In addition, RFNO is used by the 8 – bit binary counter in GAATAB as an incre – ment signal.

Note that RFNI is connected to the output of a 7407 open – collector buffer that uses RFNO as its input. The resulting logic assures that even if RFNO is LOW (inactive) a refresh request from the Expansion bus will override RFNO and a refresh cycle will be initiated.

Figure 2 – 37 shows DRAM refresh control circuit operation.

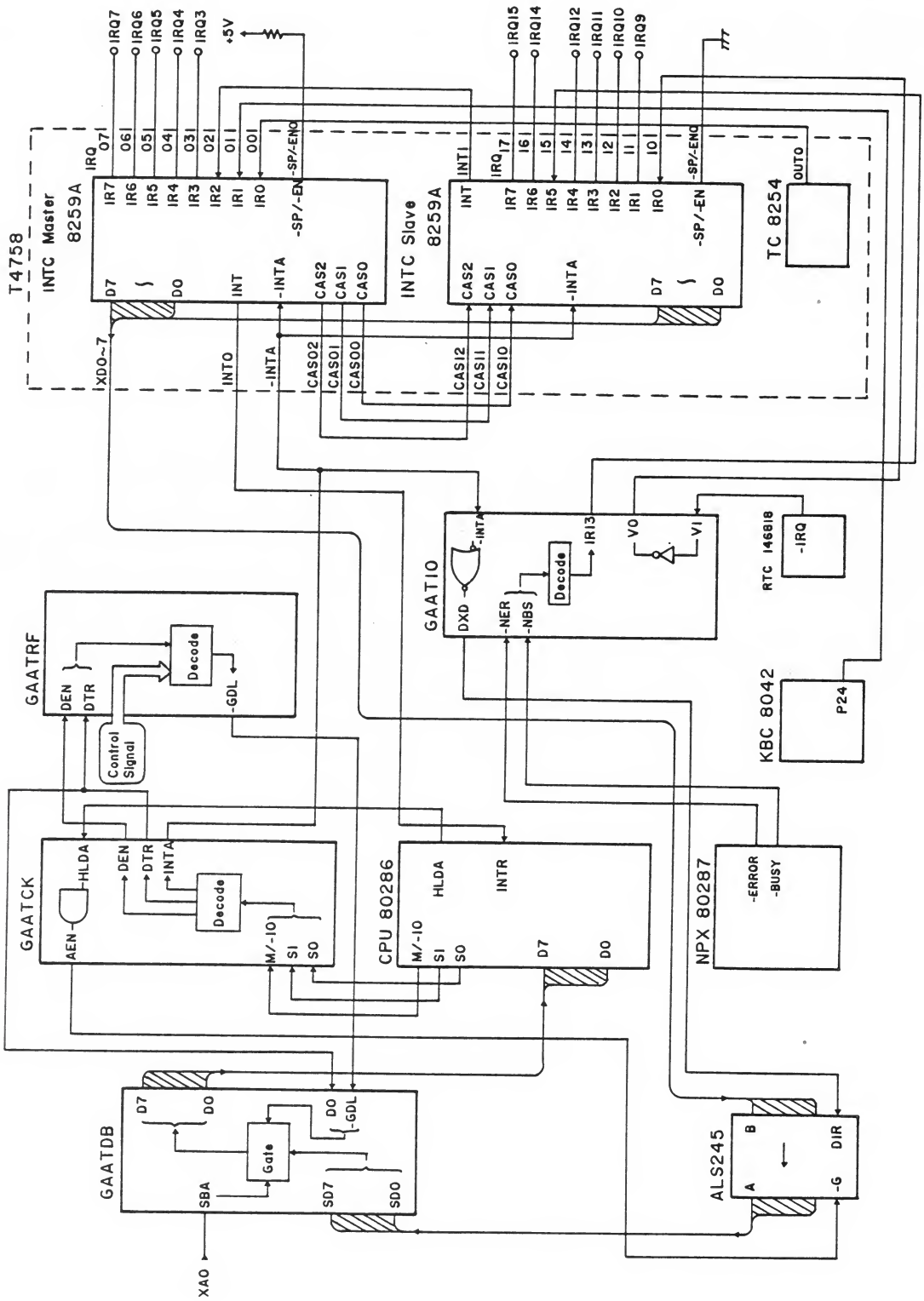


FIGURE 2 – 35. INTERRUPT CONTROL CIRCUIT

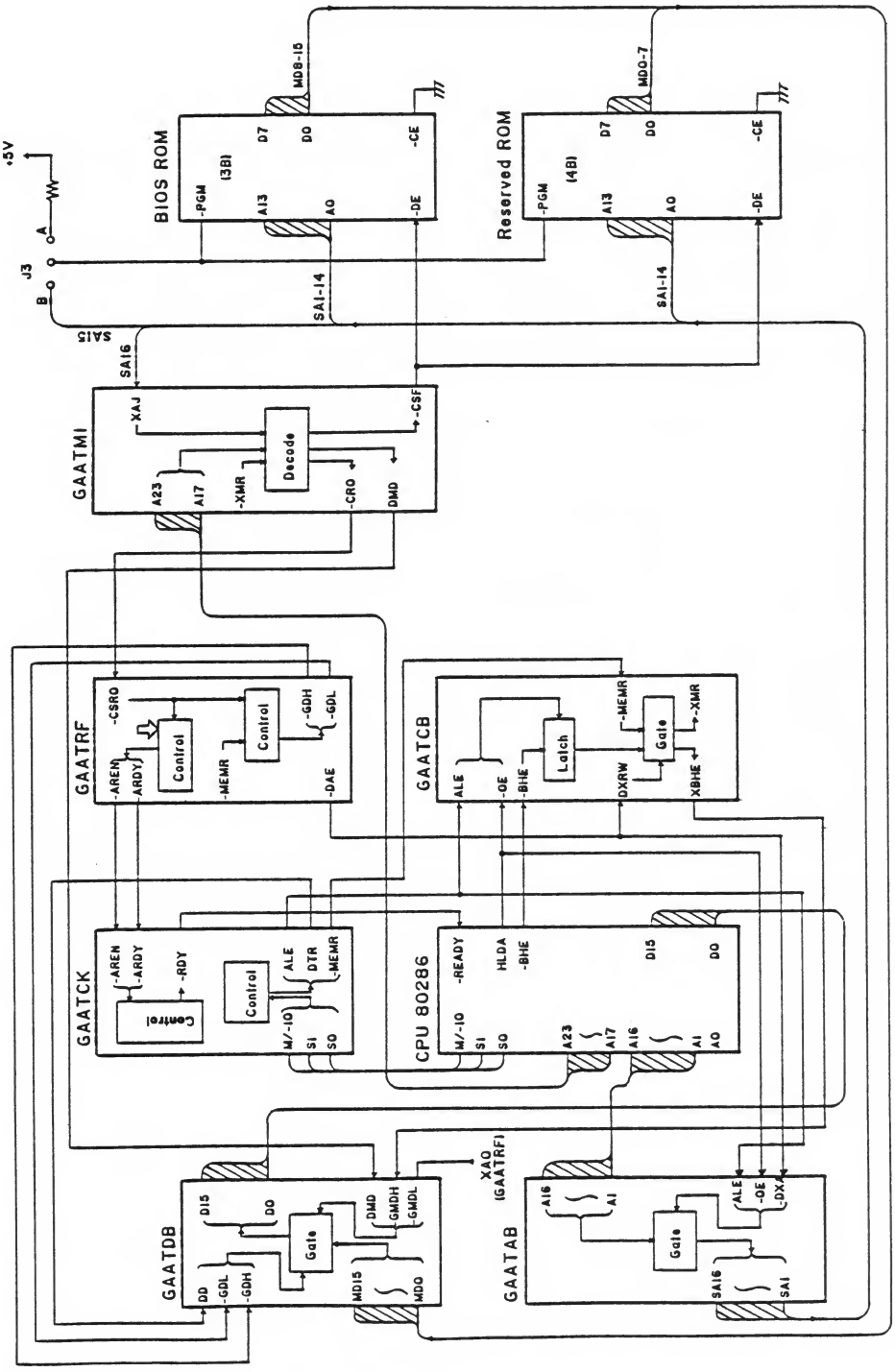


FIGURE 2 – 36. ROM ACCESS CIRCUIT

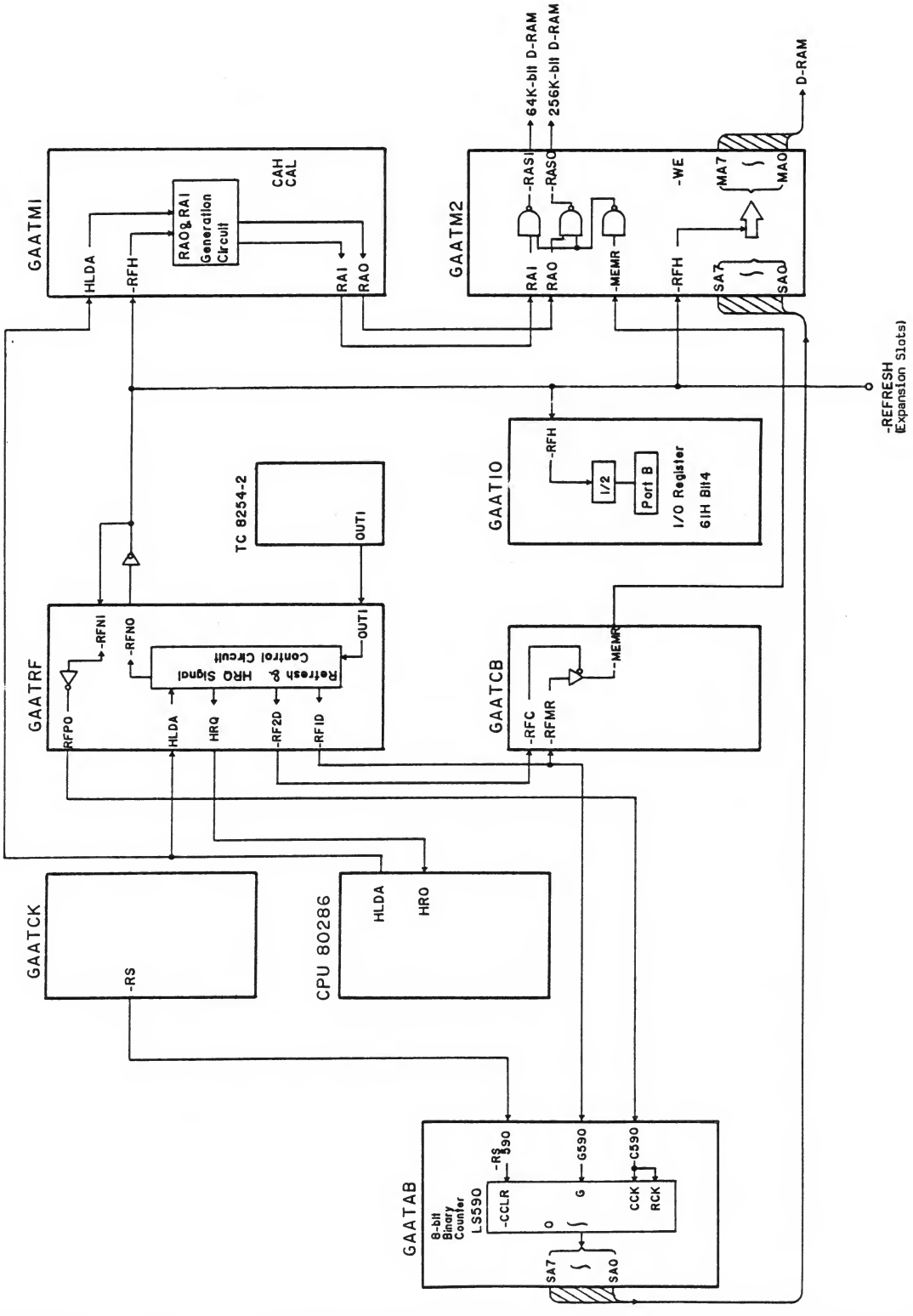


FIGURE 2 – 37. DRAM REFRESH CIRCUIT

2.3.12 RAM PARITY CHECK CIRCUIT

GAATM1 generates parity data during a DRAM write. During a DRAM read, GAATM1 compares the memory data read and the parity data. If a parity error is discovered GAATM1 outputs the – PCK signal. The GAATIO receives – PCK and generates a non – maskable interrupt (NMI) for the CPU. Figures 2 – 38 and 2 – 39 show the DRAM parity check circuit operation.

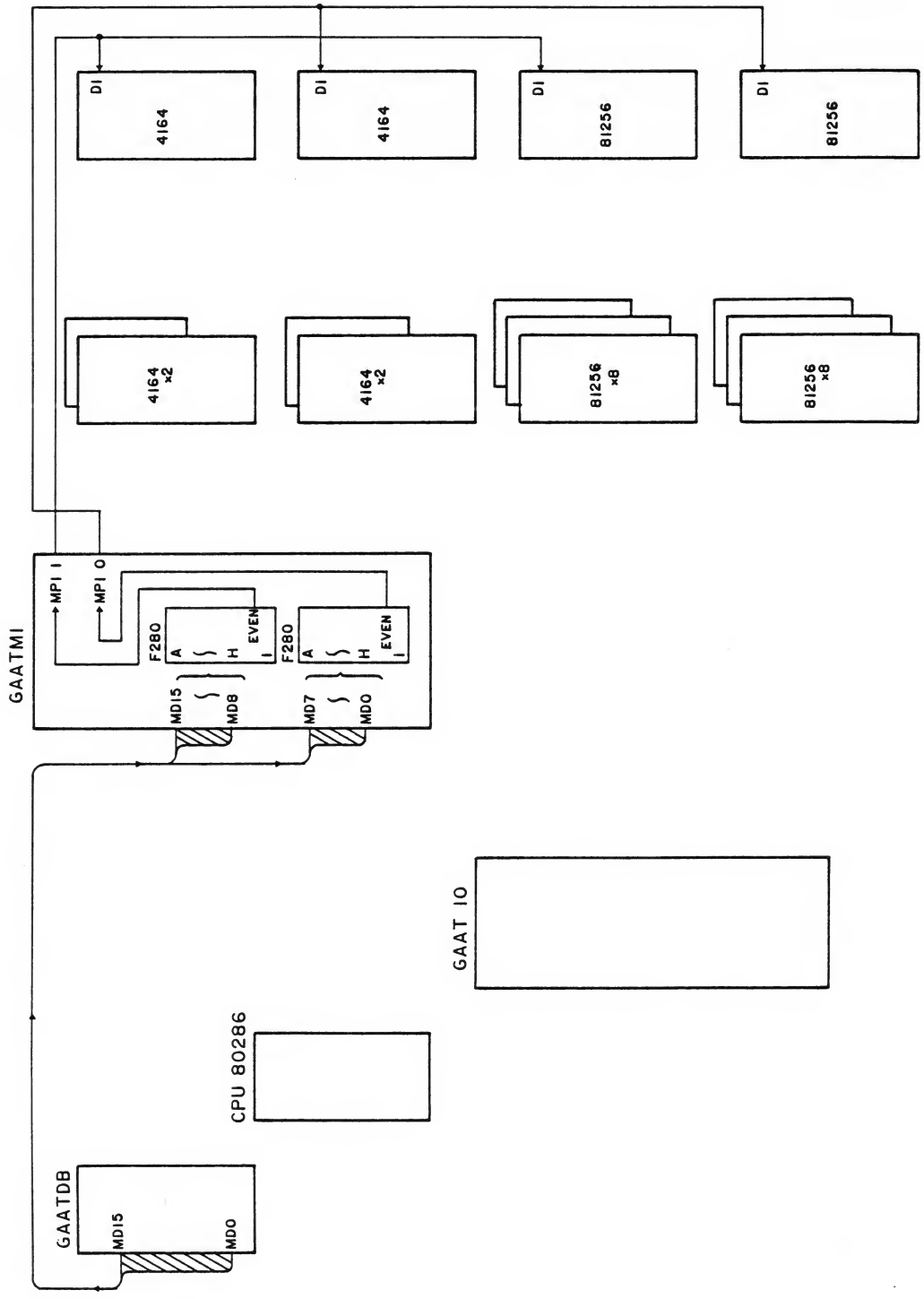


FIGURE 2 – 38. RAM PARITY CHECK CIRCUIT DATA WRITE

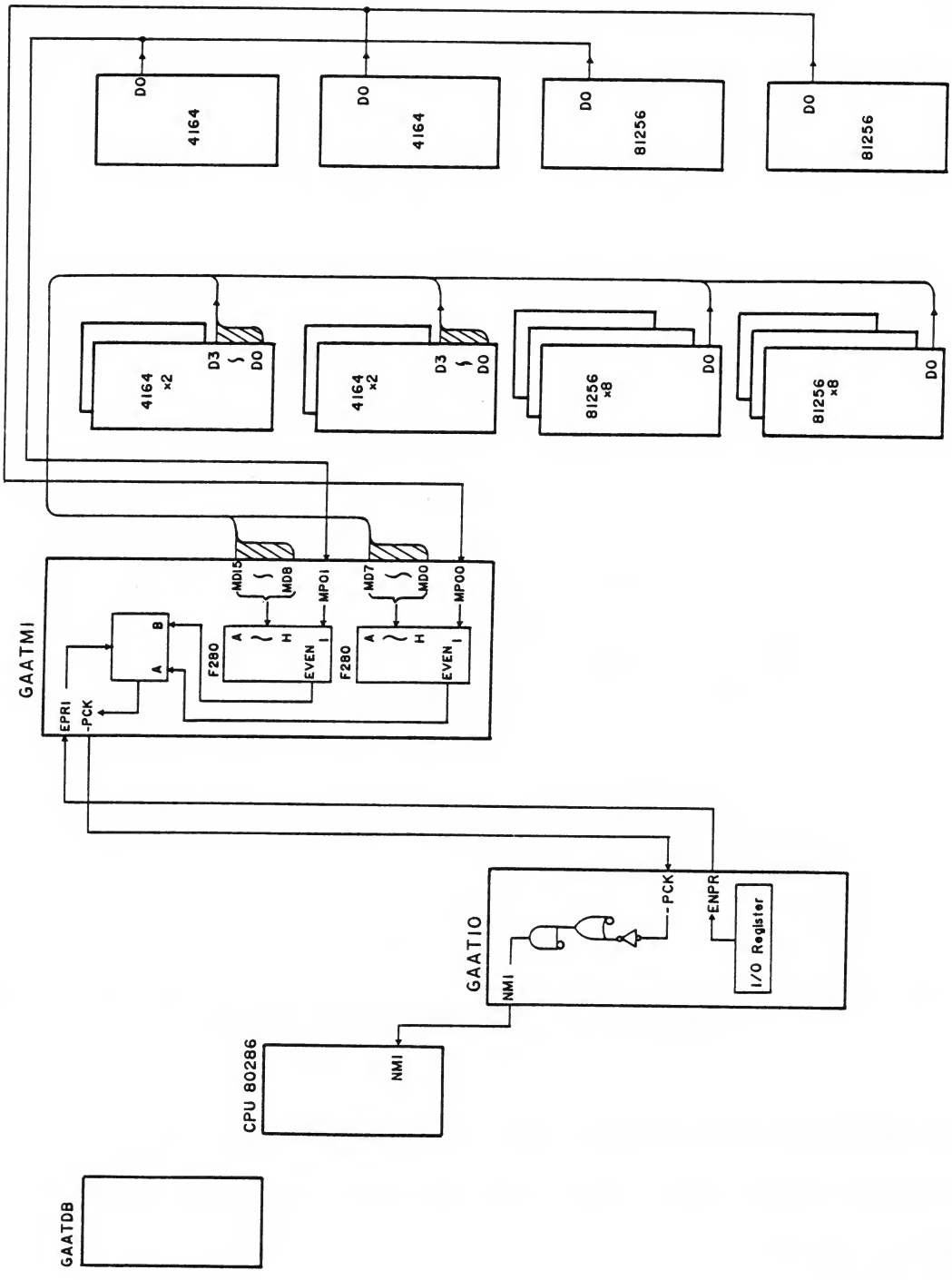


FIGURE 2 – 39. RAM PARITY CHECK CIRCUIT DATA READ

2.3.13 SPEAKER CONTROL CIRCUIT

The 8254 – 2 compatible timer/counter controls the speaker. Figure 2 – 40 shows the speaker control circuit.

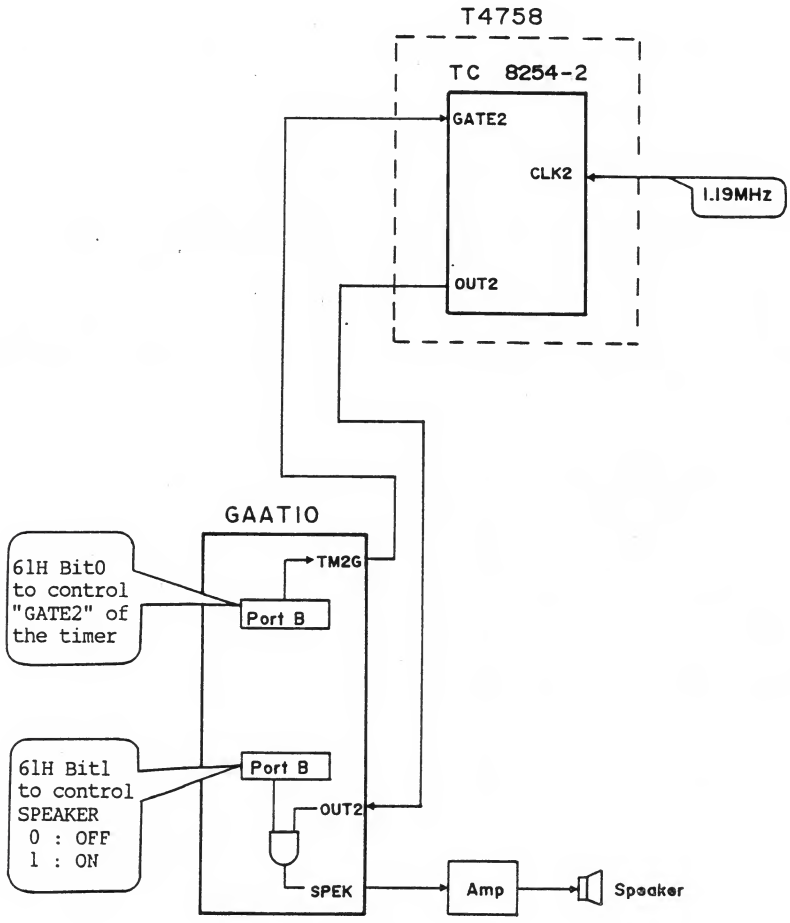


FIGURE 2 – 40. SPEAKER CONTROL CIRCUIT

2.3.14 KEYBOARD INTERFACE CIRCUIT & OTHER CIRCUITS

The keyboard controller (8042) includes circuits to perform the following functions.

1) Keyboard interface
2) RAM size read
3) Monitor type read
4) Keyboard scan code disabling
5) Software reset signal generation
6) Address A20 signal control

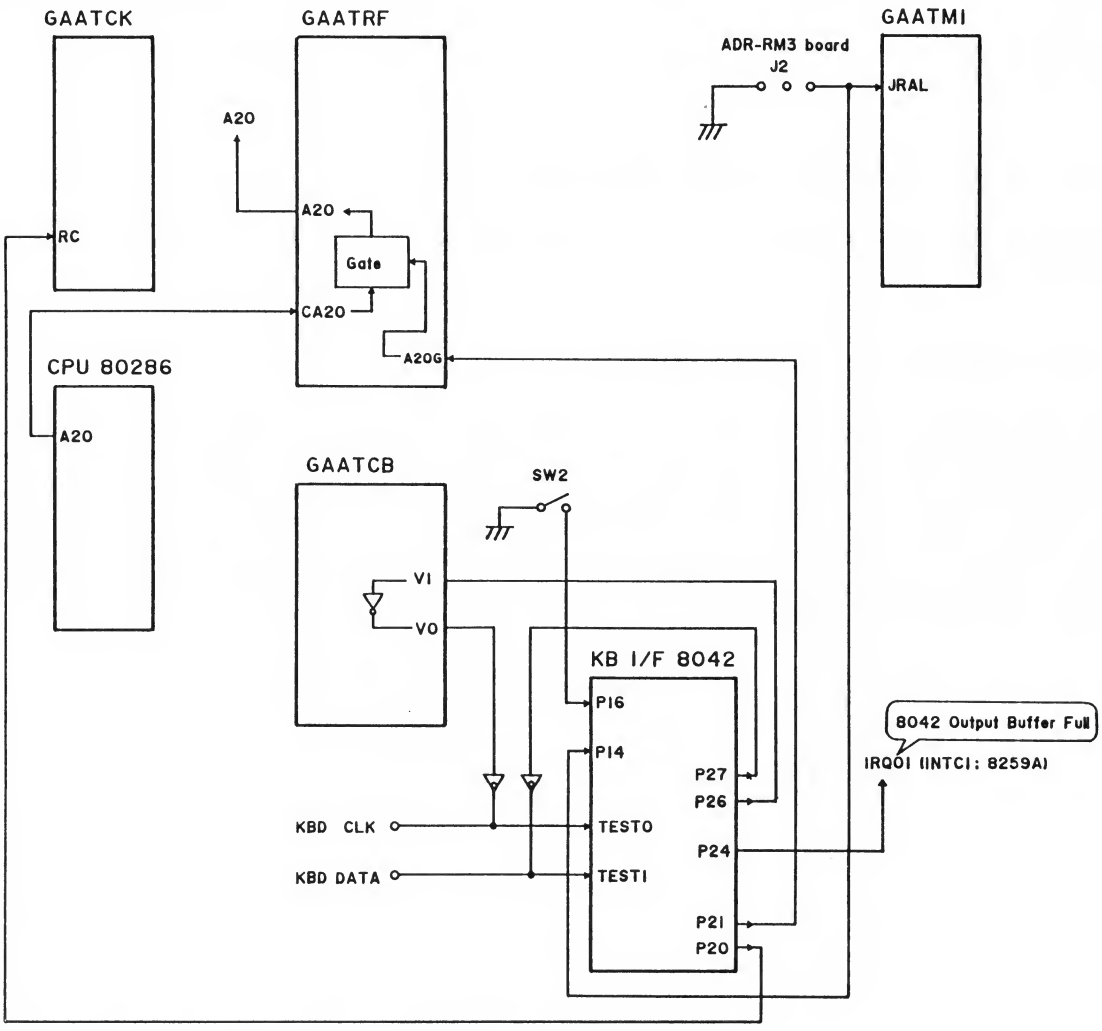


FIGURE 2-41. KEYBARD & OTHER

2.3.14.1 KEYBOARD INTERFACE

The 8042 receives keyboard data on TEST1 (pin 39). Keyboard control commands are sent from P27 (pin 38). When the 8042 receives keyboard data, it sends interrupt request signals from P24 (pin 35). P26 is used to output control signals for keyboard data transmission. For further details, see section 2.5.3.

2.3.14.2 RAM SIZE READ

The 8042 reads the condition of jumpers J2 and J3 on the ADR-RM3 / ADR-RM3S board. GAATRF works in combination with the 8042 to insure correct address-bus control.

2.3.14.3 MONITOR TYPE READING

The 8042 reads the condition of slide switch SW2 on the ANDRO board. SW2 is used to select either monochrome or color video operation.

2.3.14.4 SOFTWARE RESET SIGNAL GENERATION

The 8042 generates the software reset signal, (caused by a keyboard command, for example) from P20 (pin 21).

2.3.14.5 ADDRESS A20 SIGNAL CONTROL

The 8042 generates the A20 control (gate) signal to GAATRF. The last line of the table below represents Real Memory mode. In Real Memory mode the value of A20 from the CPU is ignored. Since the maximum addressable memory in Real mode is 1M byte, the 8042 always supplies a value of 0 (through the A20G signal) to GAATRF during Real mode operation. In Protected mode, the value of A20 can correctly be either 0 or 1. When the 80286 is in Protected mode the 8042 always outputs a value of 1 for A20G. This value is then ANDed with the CPU value for A20 (CA20), and GAATRF supplies the resulting signal (A20) to the system.

TABLE 2-14. A20 SIGNAL CONTROL BY GAATRF

CA20 From CPU	*A20G From 8042*	*A20 GAATRF Output*
0	1	0
1	1	1
*	0	0

* = Don't Care

2.3.15 I/O SLOT ACCESS SIGNALS

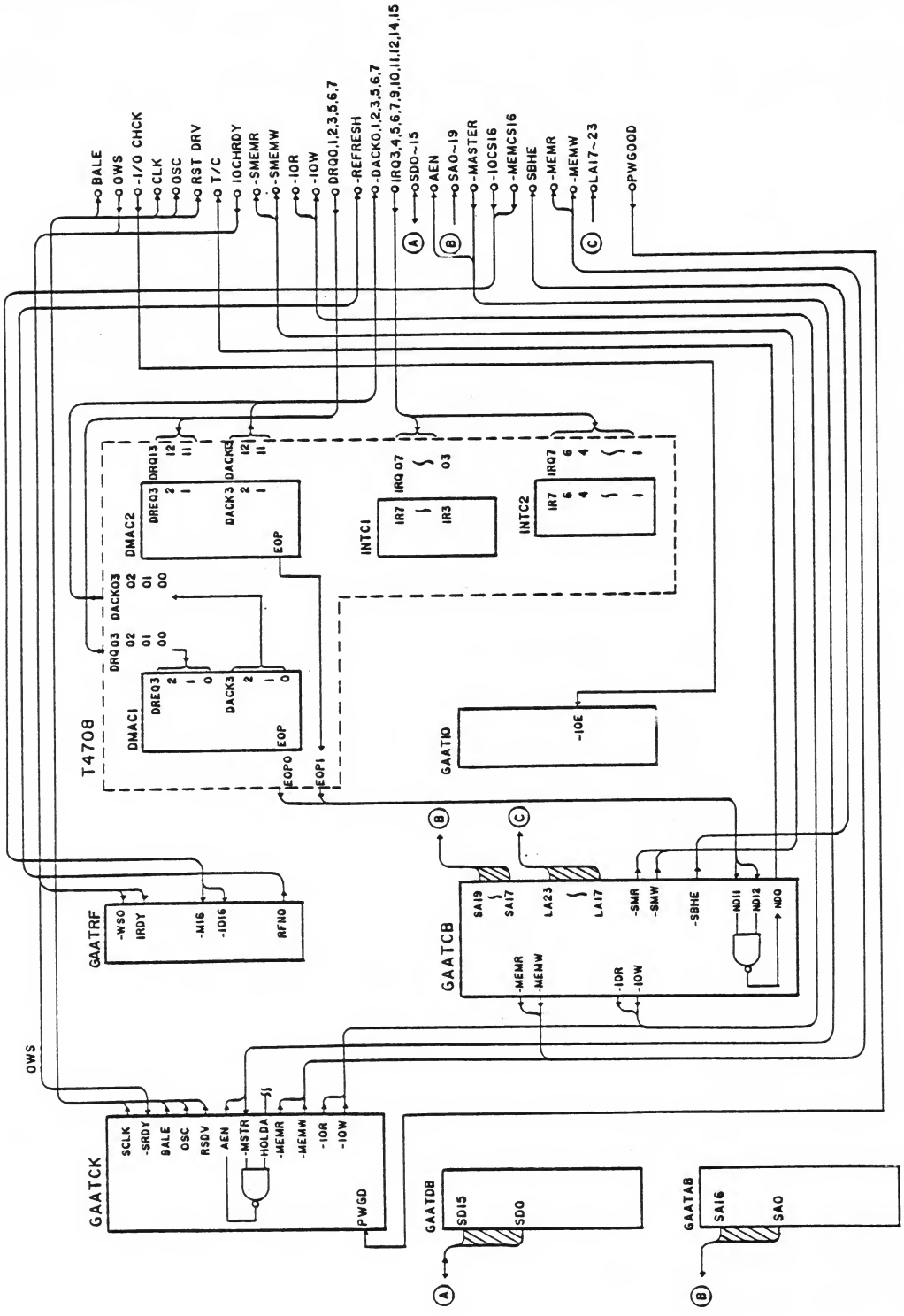


FIGURE 2-42. I/O SLOT ACCESS SIGNALS

2.4 MULTI – FUNCTION ADAPTER (SPFII BOARD)

2.4.1 SERIAL INTERFACE

An NS16450 is used as the serial communications controller. The 8250 and the 16450 are identical in function, however the data handling speed of the 16450 is higher than that of the 8250. The data transmission rate can be set as high as 56000 bps. Timing is provided by signals produced by a custom Epson gate array: the XTAL1 terminal receives a 1.8432MHz clock signal generated by the OSC terminal in the gate array GAATSP.

2.4.1.1 16450 CHIP SELECT CIRCUIT

The Chip – Select signal CS2 for activating the 16450 is supplied by gate array GAATSP (– SCS signal). There are two possible I/O addresses which the – SCS signal activates. They are selected by jumpers J5 and J6 on the SPFII board. Setting J5 and J6 to A and A assigns the serial port to I/O port address 3F8h – 3FFh. When jumpers J5 and J6 are set to A and B, respectively, the serial port is assigned I/O address 2F8h – 2FFh. Setting J5 to B will disable the serial port, regardless of the setting of J6 or J9. (In PC – compatible machines, I/O address 3F8h – 3FFh is assigned to the "primary" serial port and 2F8h – 2FFh is assigned to the "secondary" serial port. Note that the interrupt request level, set by jumper J9, must also be set to match the ap – propriate hierarchy configuration of the serial port.)

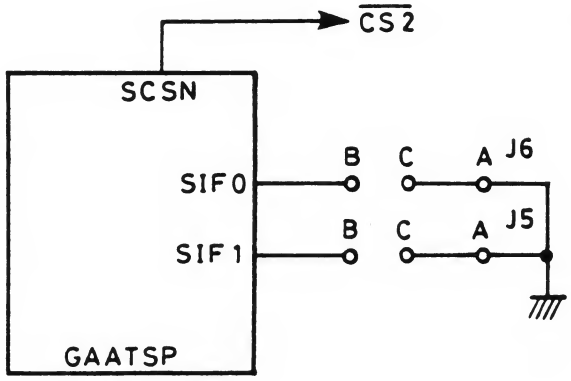


FIGURE 2 – 43. 16450 CHIP SELECT CIRCUIT

2.4.1.2 INTERRUPT SIGNAL

The Interrupt signal goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER.

1. Receiver error flag
2. Receiver data available
3. Transmitter holding register empty
4. Modem status interrupt

Output of the INTRPT signal can be applied to either IRQ3 or IRQ4. Either IRQ3 or IRQ4 is selected by jumper J9. Setting J9 to A assigns the correct interrupt request level for the "primary" serial port of the system (IRQ4). Setting J9 to B is necessary to configure the serial

port as the system's "secondary" serial port (IRQ3). Note that the serial port I/O address assignment must also be set correctly when configuring the serial port as "primary" or "secondary". (See 2.4.1.1)

TABLE 2 – 15. JUMPER J9 SETTING

J9	*INTERRUPT SIGNAL*
A	IRQ4
B	IRQ3

2.4.1.3 DATA BUFFER DIRECTION CONTROL SIGNAL

When either the serial or parallel port is read, the DDIR signal, generated by gate array GAATSP, is forced LOW.

2.4.2 PARALLEL COMMUNICATIONS CONTROL CIRCUIT

Gate array GAATSP controls the parallel communications port.

2.4.2.1 I/O ADDRESS SELECTION

There are three possible I/O port addresses to which the parallel port may be assigned, and these are selected by setting jumpers J3 and J4 on the SPFII board. Setting J3 and J4 to A and A assign the parallel port to I/O address 378h – 37Fh. Setting J3 and J4 to A and B, respectively, assigns the parallel port I/O address 278h – 27Fh. Setting J3 and J4 to B and A, respectively, assigns the parallel port to I/O address 3BCh – 3BFh. Setting both jumpers to B disables the parallel port.

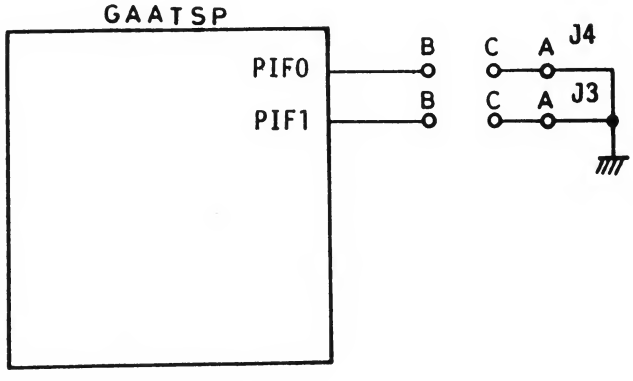


FIGURE 2 – 44. I/O ADDRESS SELECTION

2.4.2.2 PARALLEL DATA CONTROL CIRCUIT FUNCTIONS

The parallel communications control circuit has the following six functions:

1. Data output
2. Output data read
3. Printer control signal output
4. Printer control signal read
5. Printer status read
6. Interrupt signal control

Data Output Circuit

Data flow direction is one – way: from the CPU to a printer via an LS244 data latch.

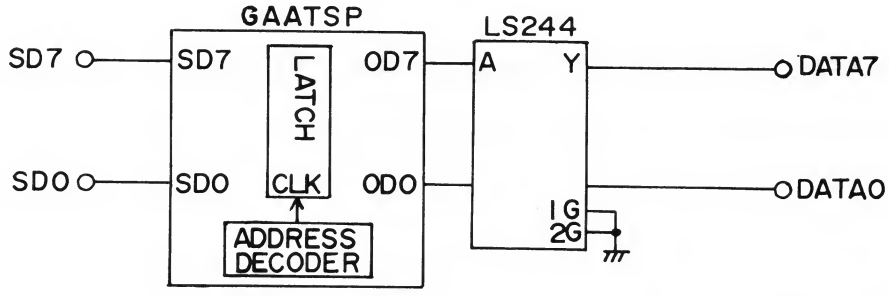


FIGURE 2 – 45. DATA OUTPUT (PRINTER DATA REGISTER WRITE)

Output Data Read Circuit

Data output to a printer can be read from the LS244 located in GAATSP.

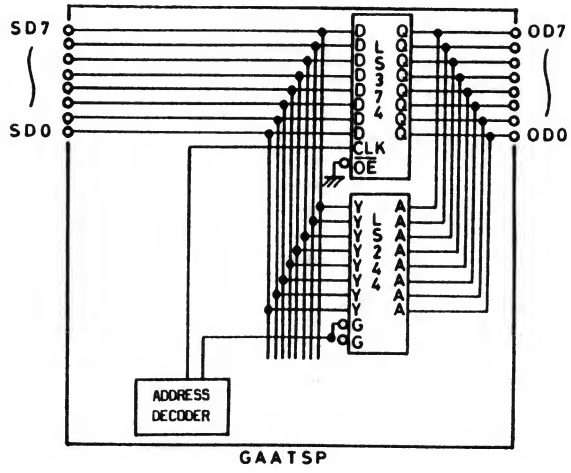


FIGURE 2 – 46. OUTPUT DATA READ CIRCUIT

Printer Control Signal Ouput Circuit

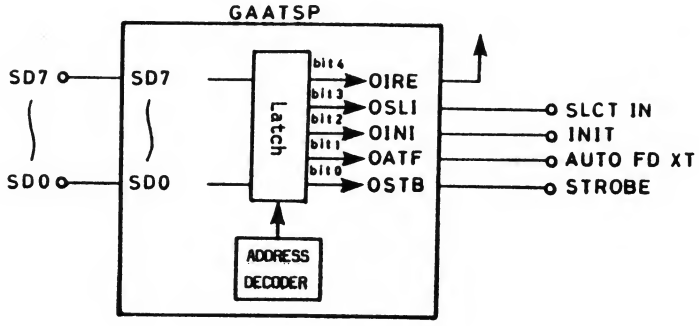


FIGURE 2 – 47. PRINTER CONTROL SIGNAL OUTPUT CIRCUIT

Printer Control Signal Read Circuit

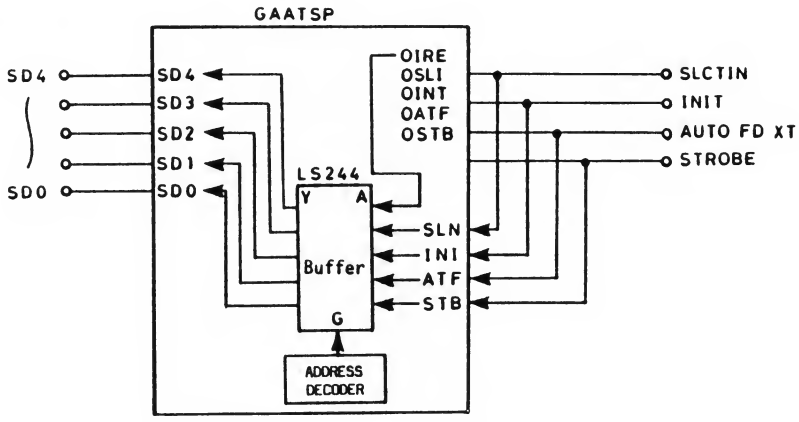


FIGURE 2 – 48. PRINTER CONTROL SIGNAL READ CIRCUIT

Printer Status Read Circuit

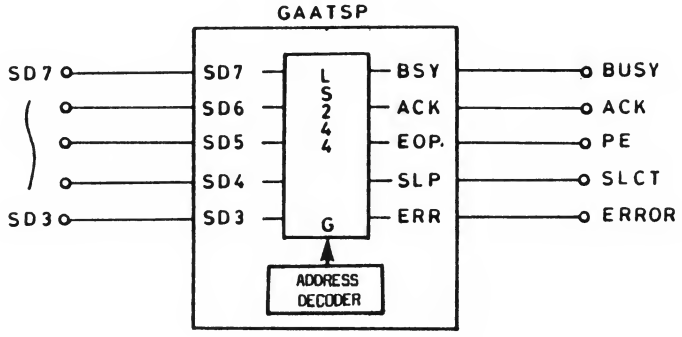


FIGURE 2 – 49. PRINTER STATUS READ CIRCUIT

Interrupt Signal Control Circuit

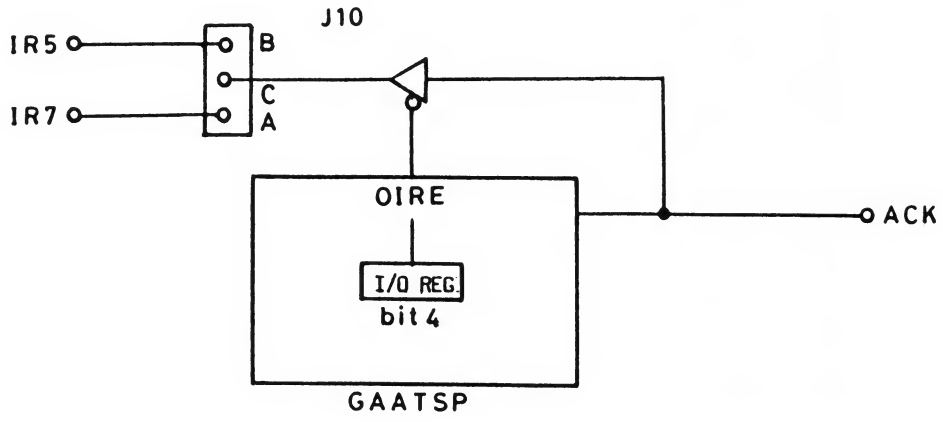


FIGURE 2 – 50. INTERRUPT SIGNAL CONTROL CIRCUIT

2.4.3 FLOPPY DISK CONTROLLER

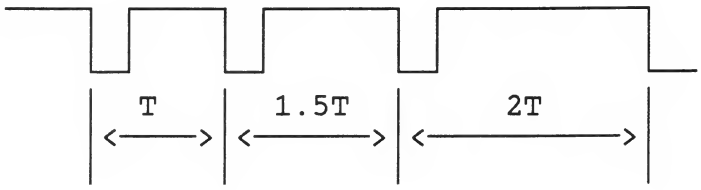
2.4.3.1 1.2MB FDD

EQUITY II / EPSON PC+ 1.2MB FDD (SD – 581L) cannot be installed on EQUITY II+ / EPSON PC AX2 because of differing FDD control signals.

TABLE 2 – 16. DIFEREENCE BETWEEN 1.2 MB FDD OF SD – 581L AND FD1155C/MD – 5501

PIN NO.	*SD – 581L (*1)*	*FD1155C/MD5501 (*2)*
2	MODE SELECT	MODE SELECT
4	DISK CHANGE	(NOT USED)
6	DRIVE SELECT 3	DRIVE SELECT 3
8	INDEX	INDEX
10	DRIVE SELECT 0	DRIVE SELECT 0
12	DRIVE SELECT 1	DRIVE SELECT 1
14	DRIVE SELECT 2	DRIVE SELECT 2
16	MOTOR ON	MOTOR ON
18	DIRECTION	DIRECTION
20	STEP	STEP
22 (*3)	WRITE DATA	WRITE DATA
24	WRITE GATE	WRITE GATE
26	TRACK 00	TRACK 00
28	WRITE PROTECT	WRITE PROTECT
30 (*3)	READ DATA	READ DATA
32	SIDE SELECT	SIDE SELECT
34	READY	DISK CHANGE
OTHER PIN	GND	GND

NOTE: (*1) SD – 581L is used in the EQUITY II/EPSON PC+.
(*2) FD1155C and MD5501 are used in the EQUITY III+/EPSON PC AX.
(*3) The difference of read/write data between SD – 581L and FD1155C / MD5501 are shown below.



NORMAL DENSITY MODE

SD – 581L: T = 4µs
FD1155C/MD5501: T = 3.33µs

HIGH DENSITY MODE

SD – 581L: T = 2µs
FD1155C/MD5501: T = 2µs

2.4.3.2 OTHER FUNCTIONS

A terminating resistor (terminator) is attached to all FDDs to provide a "dummy load". It is not necessary to remove the terminator, however, because of its high impedance (1K ohm).

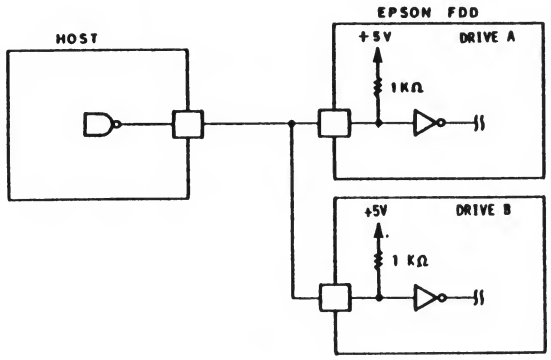


FIGURE 2 – 51. FDD TERMINATOR FUNCTION

FDD Special Signal Cable

It is not necessary to change jumper settings on the FDD in order to change the drive ID (e.g. to change FDD A: to FDD B:, and vice versa). The cable connectors determine the drive ID, so it is only necessary to exchange the cable connectors (see the diagram below).

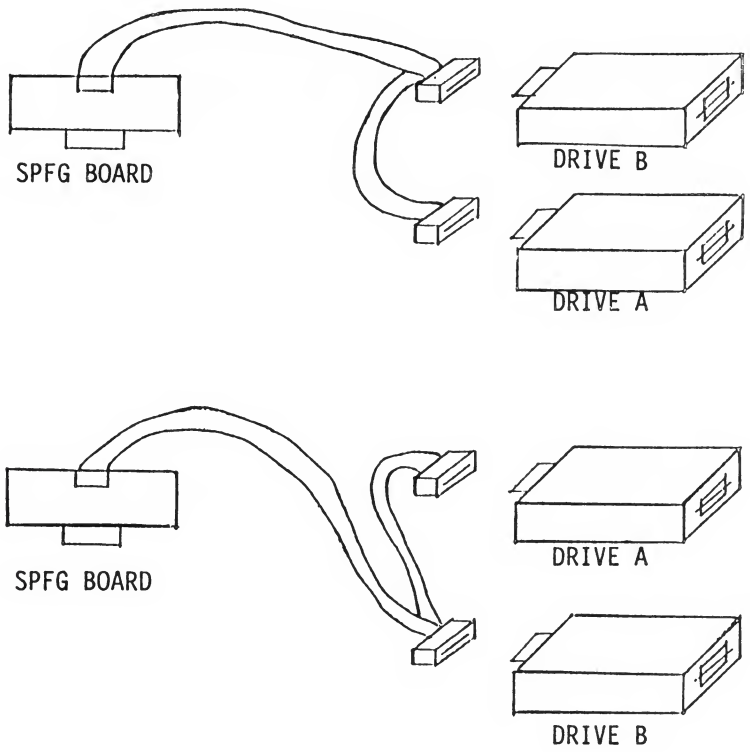


FIGURE 2 – 52. FDD CABLE CONNECTION

If the DS1 (Drive Select 1) signal is generated by the host computer, drive A is selected. If the MT1 (Motor Turn – on 1) signal is then generated, the motor in drive A is turned on.

If the DS2 signal is generated by the host computer, drive B is selected. If the MT2 signal is then generated, the motor in drive B is turned on.

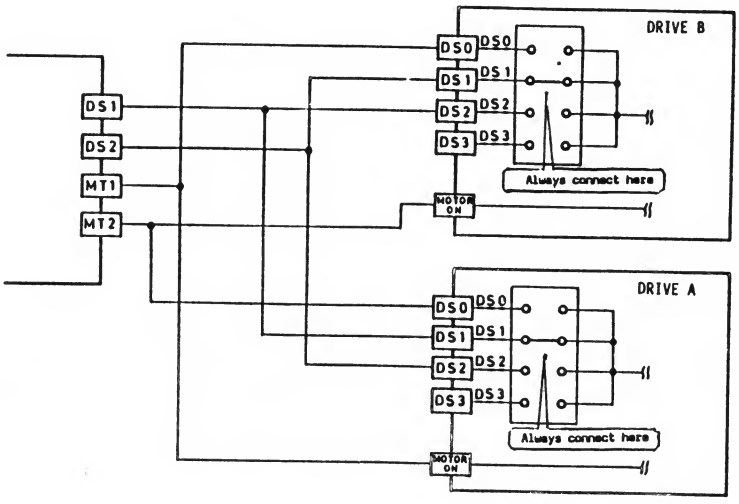


FIGURE 2 – 53. DRIVE SELECT AND MOTOR ON SIGNAL CIRCUIT

NOTE: Always set the drive select jumper switch on all FDDs to DS1 (Drive Select1).

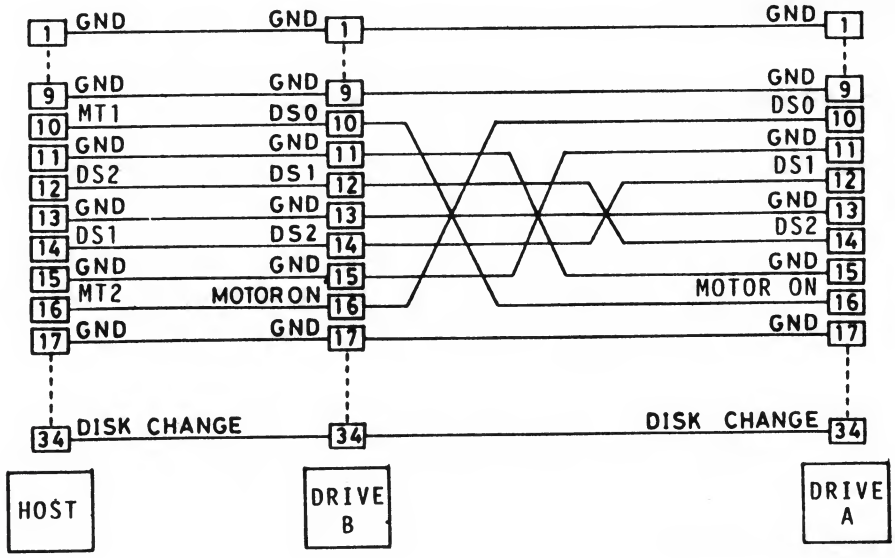
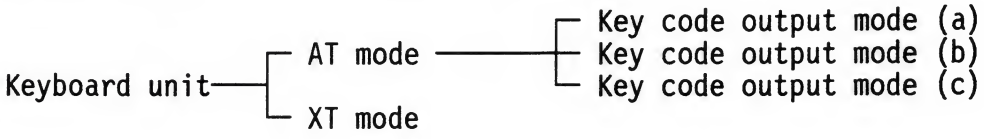


FIGURE 2 – 54. FDD SPECIAL SIGNAL CABLE

2.5 KEYBOARD

The keyboard unit has two operation modes: AT mode and XT mode.

In the AT mode, there are three different key – code output modes. Mode selection is performed by software.



The EQUITY III+ / EPSON PC AX system uses key – code output mode (b) of the AT mode.

2.5.1 BLOCK DIAGRAM

The following diagram shows keyboard unit block diagram.

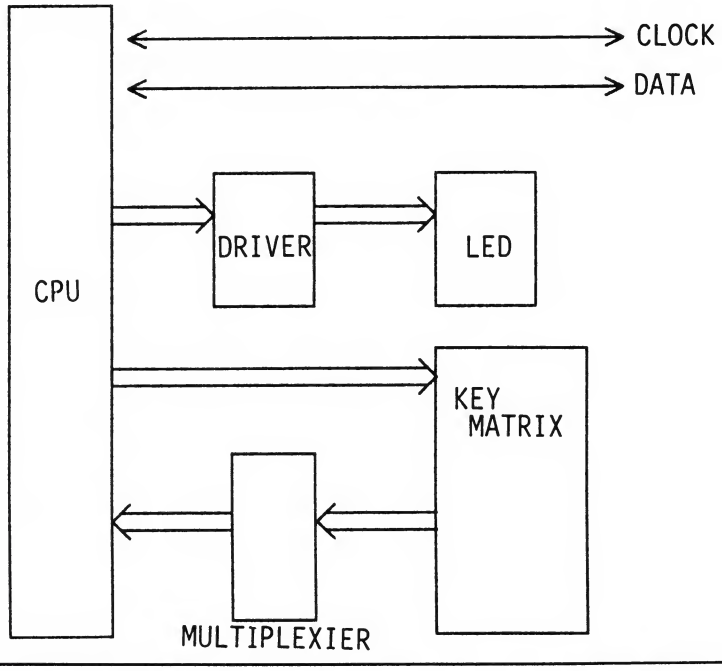


FIGURE 2 – 55. KEYBOARD UNIT BLOCK DIAGRAM

2.5.2. INTERFACE SIGNALS

AT MODE

The Keyboard data (sent from keyboard) or the keyboard control data (sent from Host side) are communicated by using the clock pin and the data signal.

There are two modes in the keyboard interface circuit. One is interface control mode, the other is data communication mode.

In the interface control mode, the host controls operation mode of the keyboard to the host or from the host to the keyboard. In this mode, the keyboard sends a clock signal to synchronize the keyboard operations and the host side operations.

TABLE 2-17. INTERFACE CONTROL MODE

CLOCK	*DATA*	*FUNCTION*
H	H	Keyboard can send Data to Host side
L	H	Keyboard can't send Data to Host side
L	L	Keyboard prepares receiving Data
H	L	Keyboard starts inputting Data

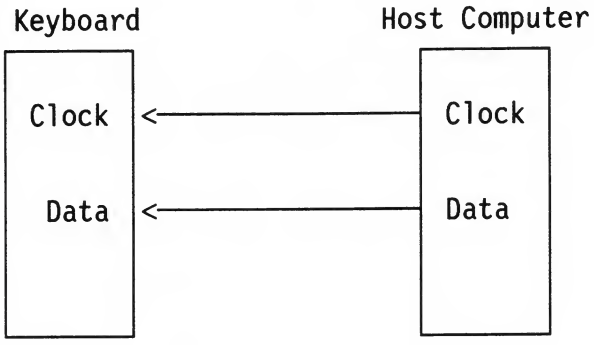
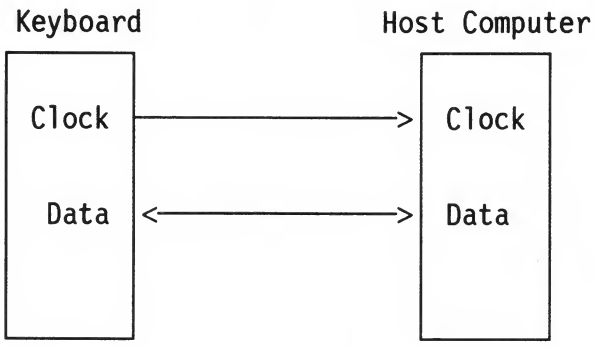


TABLE 2-18. DATA COMMUNICATION MODE (AT MODE)

CLOCK	Keyboard sends clock signal to synchronize between keyboard operation and Host side operation.
DATA	(1) Keyboard sends Data. (2) Host sends Data.



XT MODE

TABLE 2-19. DATA COMMUNICATION MODE (XT MODE)

XT	CLOCK <———	Keyboard initializing signal (low active)
	———>	Clock signal
	DATA <———	Keyboard Data wait signal (low active)
	———>	Data signal from keyboard.

2.5.3 DESCRIPTION OF INTERFACE SIGNALS (AT MODE)

2.5.3.1 CLOCK

The clock is generated by the keyboard to synchronize the transmition and reception of the keyboard data. The transmission of data cannot take place when there is a LOW clock signal (data wait) in the clock line, even if the keyboard is ready to transmit. (Data will be saved in the keyboard buffer.) The keyboard checks the clock line during the transmission of data and will stop transmission when it detects a LOW clock signal.

2.5.3.2 DATA

Data transmissions include scan codes and commands sent by the keyboard to the main unitb, and command codes sent by the main unit to the keyboard. The data signal also serves as the transmission request signal from the host. Once a LOW signal is detected in the data line the keyboard is ready to receive a command code.

2.5.3.3 KEYBOARD DATA OUTPUT (AT MODE)

When the keyboard is ready to transmit data, it checks the clock and data lines for a data wait or transmission request. When both the clock and data lines are HIGH, the keyboard starts transmitting. During transmission, the keyboard samples the clock line and stops data transmis-sion as soon as it detects a low level signal.

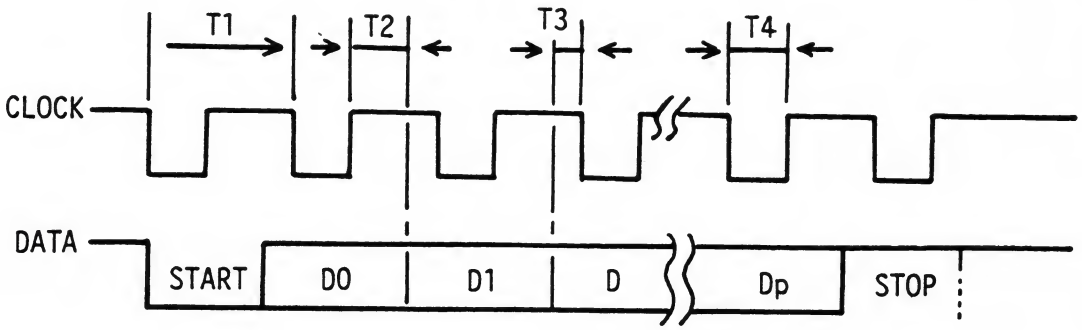
2.5.3.4 KEYBOARD DATA INPUT (AT MODE)

When the keyboard detects a low level signal in the data line it prepares to receive a command code from the main unit. When host clock signal then goes LOW for at least 60 µs the keyboard stops transmitting. The keyboard then waits for the clock line to go HIGH, and data reception is performed in groups of 11 bits. After receiving the 10th bit of each group the keyboard forces the data signal LOW and receives one more bit (the stop bit). The LOW signal for the 11th bit tells the main unit that the data has been received.

2.5.3.5 DATA TRANSMISSION METHOD AND DATA FORMAT

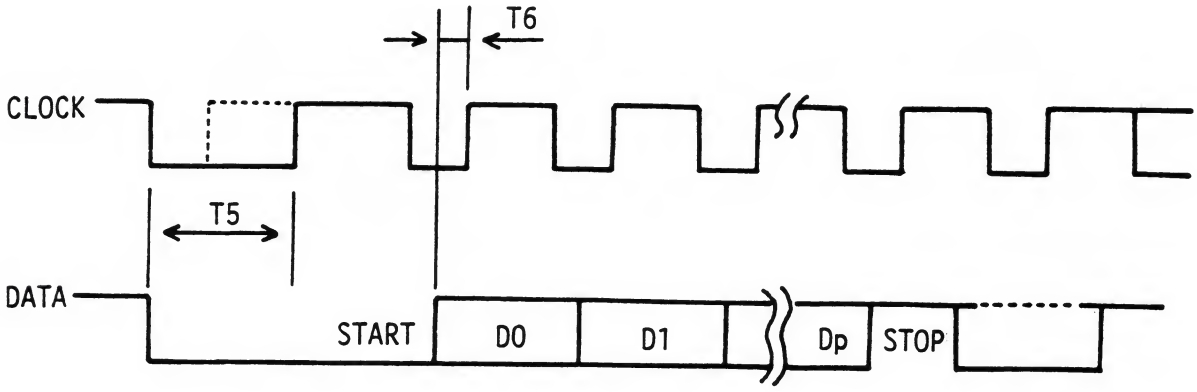
TABLE 2-20. DATA TRANSMISSION METHOD AND DATA FORMAT

	AT Mode	*XT Mode*
(1) Transmission method	Synchronous serial transmission	Synchronous serial transmission
(2) Transmission rate	9600bps	9600bps
(3) Start bit	1	1
(4) Stop bit	1	1
(5) Data length	8 bit	8 bit
(6) Parity	Odd parity	None



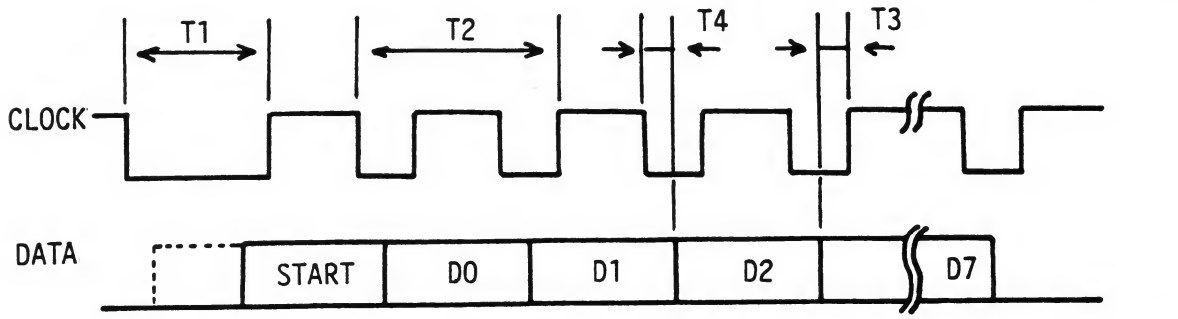
T1 ; 104 us ±20%
T2 ; 20 us Min
T3 ; 20 us Min
T4 ; 35 us ±20%

FIGURE 2-56. KEYBOARD DATA OUTPUT - AT MODE



T5 ; 60 us Min (Host data output ready time)
T6 ; 5 us Min

FIGURE 2-57. KEYBOARD DATA INPUT - AT MODE



T1 ; 100 - 250 us (Data output possibility
T2 ; 104 us ±20% check time)
T3 ; 10 us Min
T4 ; 10 us Min

FIGURE 2-58. KEYBOARD DATA OUTPUT - XT MODE

2.5.4 INTERFACE CIRCUIT SPECIFICATION

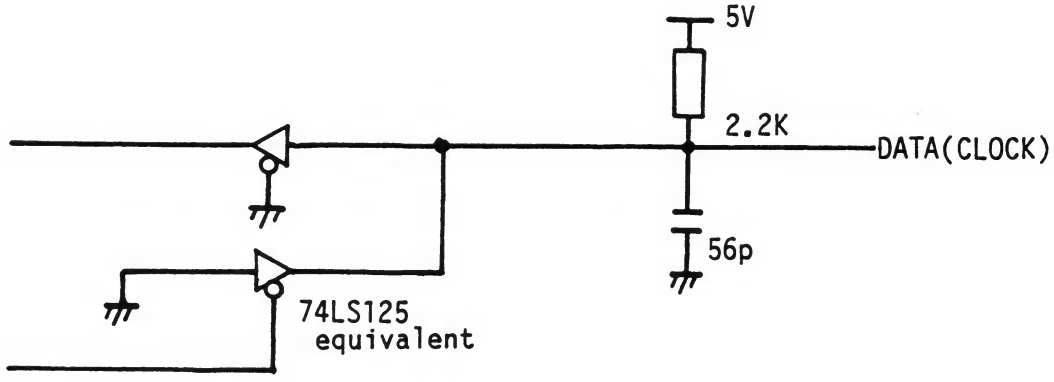


FIGURE 2-59. INTERFACE CIRCUIT

2.5.5 CONNECTOR PIN EXPLANATION

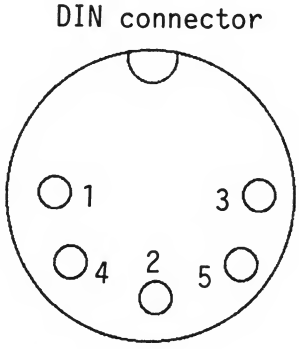


FIGURE 2-60. KEYBORAD CONNECTOR PIN LOCATIONS

TABLE 2-21. KEYBOARD CONNECTOR PIN FUNCTION

Pin Number	*Signal Name*
1	Clock
2	Data
3	N.C.
4	Ground
5	+5V DC
–	Ground

2.5.6 FUNCTION SPECIFICATIONS

2.5.6.1 STROKE CHARACTERISTIC

The stroke characteristic of the keyboard is called Scroll Over (similar to N-key Roll Over).

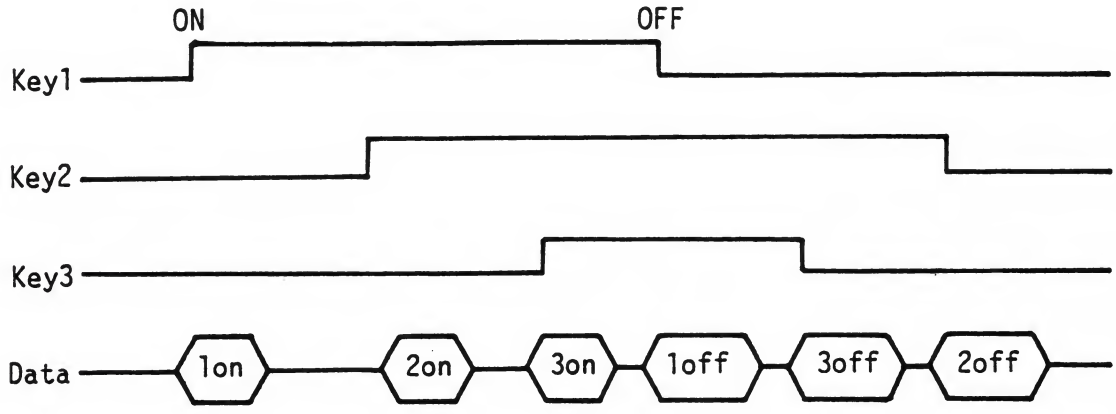


FIGURE 2-61. STROKE CHARACTERISTICS

2.5.6.2 TYPEMATIC FUNCTION

A key scan code is transmitted as long as a key is depressed. (Transmission intervals for all keys except the F16 (Pause) key depend on the typematic rate/delay (command assignment). When any of the other keys are pressed, a new typematic cycle is entered.

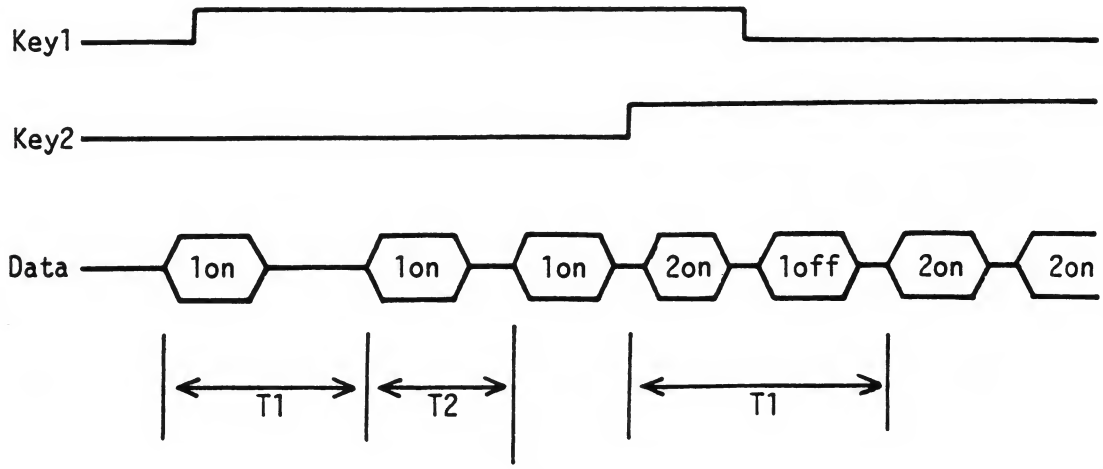


FIGURE 2-62. TYPEMATIC FUNCTION

TABLE 2-22. TRANSMISSION INTERVALS

AT Mode	*XT Mode*
T1 250 - 1000 ms (default)	500 ms
T2 1/2 - 1/3 sec (default)	92 ms

NOTE: The typematic function will be disabled when the clock line is LOW.

2.5.6.3 KEYBOARD BUFFER

When a key is pressed (released) before the code of a key pressed earlier has been transmitted during the key data out phase, the code of the non-transmitted key is saved in this buffer until it is transmitted. The buffer can save codes for 16 keys (16 make or break data). The 17th code will be substituted by an overrun code. However, no substitution will take place if there is an overrun code in the buffer.

Break codes and make codes created when a key is depressed will not be lost even during an overrun. However, they will be cancelled by a buffer clear command. The overrun code is different for the AT mode and XT mode, as shown below.

TABLE 2-23. OVERRUN CODES

Key Code Output Mode	*(a)*	*(b)*	*(c)*
AT mode	FF	00	00
XT mode		FF	

2.5.6.4 POWER ON RESET (AT MODE)

When the power is turned on the keyboard logic performs a power-on reset.

(1) Following the power on reset, a self-test program is performed.

. ROM check sum self-test program
. RAM checkself-test program

(2) After the test, the keyboard turns off the mode indicator display (3 LED's) and transmits the end code of the self-test program.

. "AAH": operated correctly
. "FCH": operated abnormally (scanning is stopped after transmission of the end code.)

(3) When the operation normal end code (AAH) has been transmitted and the keyboard detects a low level signal longer than 10µs in the data line 5µs after from following edge of the stop bit, the keyboard enters the XT mode.

(4) In AT mode, the typematic rate/delay time and key code output mode will be set according to mode (b).

. Rate : 10.9 CPS (92 ms) Default
. Delay : 500 ms Default

2.5.6.5. INITIALIZING (XT MODE)

The clock line is checked in 10ms cycles by keyboard and initialization is performed as soon as a LOW signal is detected.

(1) Key scan memory clear

(2) Buffer (FIF0) clear

(3) Self – test program performed

. ROM sum check self – test program
. RAM check self – test program

(4) Transmission of self – test program end code

. "AAH": Operated correctly
. "FCH": Operated abnormally (scanning is stopped after transmission of the end code.)

2.5.6.6 DATA WAIT FUNCTION (XT MODE)

When the start bit is set, the data line is checked by the keyboard and if a LOW signal (longer than 250µs) is detected in the data line, data transmission will not take place.

2.5.6.7 MODE INDICATOR (3 LED'S) DISPLAY (XT MODE)

Basic Operation

(1) By pressing the Scroll Lock, Numeric Lock and Caps Lock keys each indicator is displayed alternatively (performed after the end of key code transmission).

(2) All displays are turned off during power on reset and initialization.

(3) The alternative operation does not take place when the control (Ctrl) key is pressed.

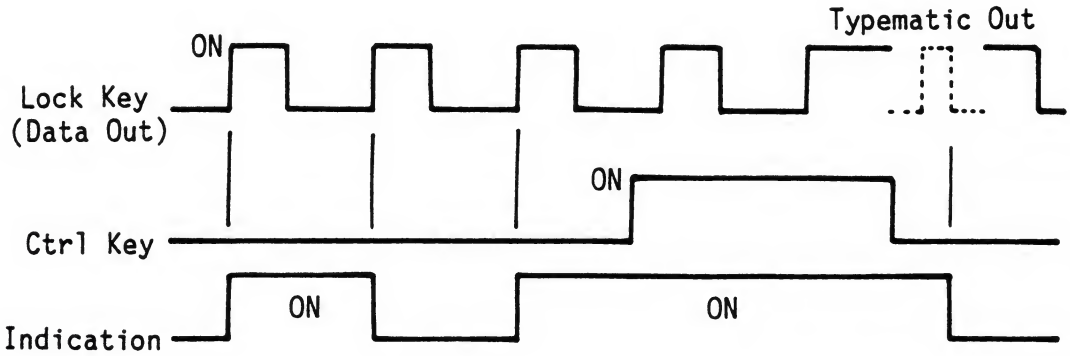


FIGURE 2-63. BASIC OPERATION OF MODE INDICATOR DISPLAY

Special Operations (For German and French Keyboards)

By pressing the Caps key, Caps Lock indicator becomes on (light). By pressing the shift key, Caps Lock indicator becomes off (Not light).

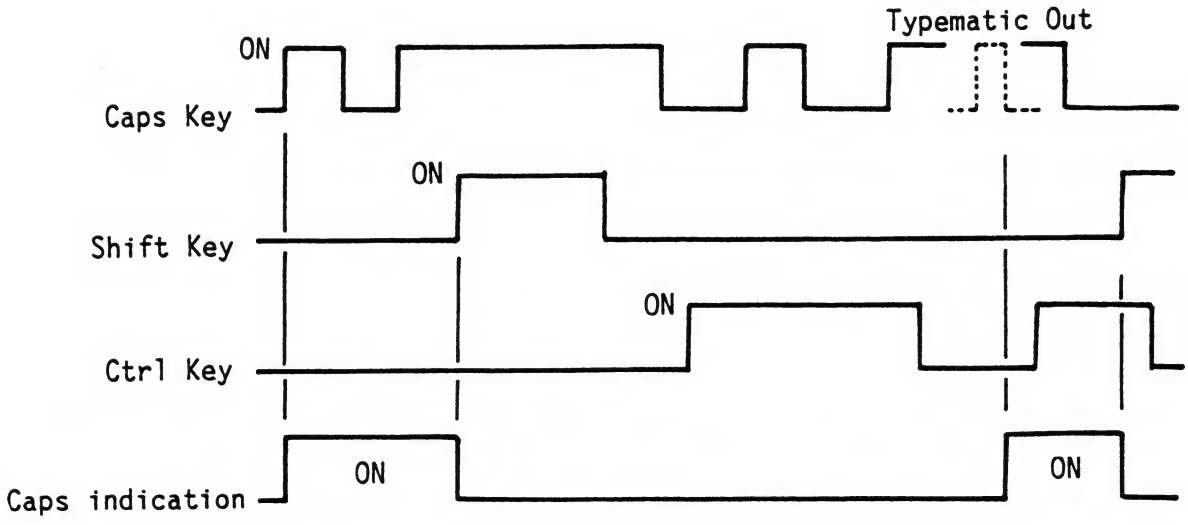


FIGURE 2-64. SPECIAL FUNCTIONS OF MODE INDICATOR DISPLAY

2.5.7 KEY SCAN CODE

2.5.7.1. KEY CODE OUTPUT IN AT MODE

In AT mode, there are three output modes: (a), (b) and (c)

Key code output in mode (a) and (b)

(1) Key code make up: The table below shows the codes allocatted to each key.

TABLE 2-24. KEY CODE MAKE UP

Title	*Key Position*	*Make Code*[1]		*Break Code*[2]	
		Mode (b)	*Mode (a)*	*Mode (b)*	*Mode (a)*
General Keys	Other	x	x		
	A09, B20, A12	E0 + x	E0 + x		
Extension Key-1	A, D, E14-E16 B15	E0 + x	E0 + x	Make code is substituted by "F0 + x".	"80" is added to make code "x" (OR).
Extension Key-2	E18	E0 + x	E0 + x		
Extension Key-3		E0 + x	E0 + x		
Shift Key	B00, B11	x	x		
Special Key	F16 (Pause)	8 bytes	6 bytes	No key code output	

[1] Code transmitted when key is pressed.
[2] Code transmitted when key is released.

Note 1 : The "x" code indicates scan code data. (Refer to Table 2-5-22)
Note 2 : The F14 and 16 keys can generate other codes if used in combination with other keys. (Refer to section 2.5.7.1)

(2) Shift function

a) Num Lock: The table below shows the conditions for setting and releasing the numeric lock.

TABLE 2-25. CONDITION FOR SETTING AND RELEASING NUMERIC LOCK

Set	When the E17 (Num lock) is pressed and the make code has been transmitted or when the Num Lock LED been lit by a host command while the numeric lock is in released status.
Released	When the E17 key (Num lock) is pressed and the make code has been transmitted or when the Num Lock LED has been turned off by a host command while the numeric lock is in set status.

Note 1: When the A00 or the A12 key (Ctrl) are pressed, it is not possible to perform setting or releasing with the Numlock key. (Setting and releasing cannot be performed even if the Ctrl key is released first.)

b) Extension Left and Right shift key code transmission

TABLE 2-26. EXTENSION SHIFT KEY-STROKE CONDITIONS

Mode	*Extension Shift Set*	*Extension Shift Released*
Not Num Lock	Extension shift off code is transmitted when extension key-1 (or extension key-2) is pressed after the shift key has been pressed. When extension key-2 is pressed the same operation is performed even in Num Lock mode	(1) Extension-Shift-On code is transmitted when extension key-1 or extension key-2 is released. (2) Extension-Shift-On code is transmitted when other keys are pressed.
Num Lock	Extension-Left-Shift-On code is transmitted when extension key-1 or extension key-3 is pressed after the shift key has been pressed. When extension key-3 is pressed, the same operation is performed, even when not in Num Lock mode.	(1) Extension-Left-Shift-Off code is transmitted when extension key-1 or extension key-3 is released. (2) Extension-Left-Shift-Off code is transmitted when other keys are pressed.

TABLE 2-27. EXTENSION LEFT AND RIGHT SHIFT CODES

Type		
Extension Left Shift On code	E0 + 12	E0 + 2A
Extension Left Shift Off code	E0 + F0 + 12	E0 + AA
Extension Right Shift On code	E0 + 59	E0 + 36
Extension Right Shift Off code	E0 + F0 + 59	E0 + B6

TABLE 2-28. TRANSMISSION SEQUENCE OF LEFT AND RIGHT CODES KEY

Condition	*Transmission Sequence*
Extension Shift Set	EXS ——————> x
Extension Shift Release:	
When Extension Shift Setting key is OFF	x ——————> EXS
When other keys are ON	EXS ——————> x

Note: "x" = Key data
"EXS" = Extension Left and right shift codes

(3) Special operations generated by a combination of keys

a) The codes shown in the table below are transmitted when the F16 (Break) key is pressed while either the A00 (left Ctrl) or the A12 (right Ctrl) key is also pressed.

TABLE 2-29. TRANSMITTED CODE OF F16 (BREAK) KEY

Mode (b)	E0 + 7E + E0 + F0 + 7E
Mode (a)	E0 + 46 + E0 + C6

(4) Key code output during typematic operation

All keys except the F16 (pause) key are typematic keys whose make codes are transmitted at specified intervals.

TABLE 2-30. TRANSMITTED CODE OF F14 (Sys Rq) KEY

Mode	When A00 or A12 AND B00 or B11 Keys Pressed (Any Ctrl + Shift) Make	Break	When A01 or A09 are pressed (Any Alt)	
(b)	E0 + 7C	E0 + F0 + 7C	84	F0 + 84
(a)	E0 + 37	E0 + B7	54	D4

Note: No codes shown above are transmitted when the F14 (Sys Rq) key is pressed while the [A01 (left Alt), the A09 (right Alt)] and the [A00 (left Ctrl), A12 (right Ctrl)] key or the B00 (Left shift) and B11 (right shift) keys.

Key Code Output in Mode (c)

(1) Transmission of make codes (when keys are pressed): A one byte make code is transmitted when a key is pressed (refer to scan code table).

(2) Transmission of break codes (when keys are released): The A00 (left Ctrl), the A01 (left Alt), the B00 (left shift), the B11 (right shift) and the C00 (Caps) keys transmit break codes when a key is released. The break code is "F0 + make code".

(3) Key code output during typematic operation: The A04, A14 – A16, B01 – B10, B15, C01 – C12, D00 – D14, E00 – E13, D20,E13', C12', B11', B00' and D20' keys are typematic keys whose make codes are transmitted at specified intervals when pressed repeatedly.

(4) The break code transmission keys in (2) and the typematic keys in (3) above are set during default and all keys can be set with the commands described below.

2.5.7.2 KEY CODE OUTPUT IN XT MODE

The Key code outputs are performed according to the same conditions that prevail in key code mode (a) during AT mode (including shift function).

2.5.8 COMMANDS (AT MODE)

2.5.8.1 COMMANDS FROM THE HOST SIDE

These are commands received by the keyboard which it responds to within 20ms.

TABLE 2-31. KEYBOARD COMMANDS (AT MODE)

Command	*Data (Hex)*	*Buffer Clr*	*LED Set*
Reset	FF	Y	Y
Resend	FE	N	N
Typematic Key Reset 1, 2	FC, FD	Y	N
Typematic Key Set	FB	Y	N
All Key Typematic Control	FA-F7	Y	N
Set Default	F6	Y	N
Default Disable	F5	Y	N
Enable	F4	Y	N
Set Typematic Rat/Delay	F3	N	N
Read Keyboard ID	F2	N	N
Set/Read Key Code Mode	F0	Y	N
Echo	EE	N	N
Set/Reset Mode Indicators	ED	N	Y

Reset
The keyboard recognizes this command with the acknowledge (ACK) command. When reception of the ACK command has been confirmed (confirmation is mode when both the clock and data line signals exceed 500 us high) a reeset operation indentical with the power on reset is performed. (Except for XT mode switching operation)

Resend
The keyboard repeats the transmission of end data transmitted when recives a resend command.

Set default
The keyboard responds with an ACK command and continues scanning after the output buffer has been cleared and the default condition has been set.

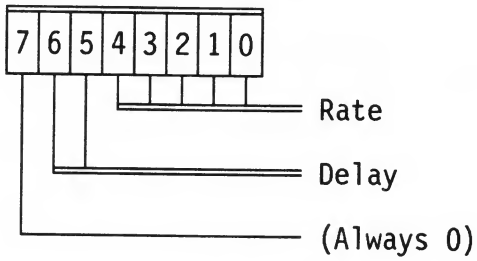
Default disable
The keyboaed stops scanning and except that it waits for a command it behaves as during a set default command.

Enable
The keyboard acknowledges to the host side with and ACK command and clears the output buffer. Then starts scanning.

Set typematic Rate/Delay
This command is made up of a 2-byte command and parameter.
The keyboard responds to the ACK command, stops scanning and waits for the parameter. Then the keyboard responds to the parameter with an ACK command, sets the rate and

delay shown in the figure below and starts scanning (when proceeded as an Enable). If a command is received instead of a parameter, the current rate remains unchanged and keyboard stops this command operation, then the new command is performed and scanning starts.

TABLE 2-32. TYPEMATIC RATE/DELAY



Typematic Rate (in CPS)

Bit	Rate	Bit	Rate	Bit	Rate
00000	= 30.0	01011	= 10.9	10110	= 4.3
00001	= 26.7	01100	= 10.0	10111	= 4.0
00010	= 24.0	01101	= 9.2	11000	= 3.7
00011	= 21.8	01110	= 8.6	11001	= 3.3
00100	= 20.0	01111	= 8.0	11010	= 3.0
00101	= 18.5	10000	= 7.5	11011	= 2.7
00110	= 17.1	10001	= 6.7	11100	= 2.5
00111	= 16.0	10010	= 6.0	11101	= 2.3
01000	= 15.0	10011	= 5.5	11110	= 2.1
01001	= 13.3	10100	= 5.0	11111	= 2.0
01010	= 12.0	10101	= 4.6		

Delay (in ms)

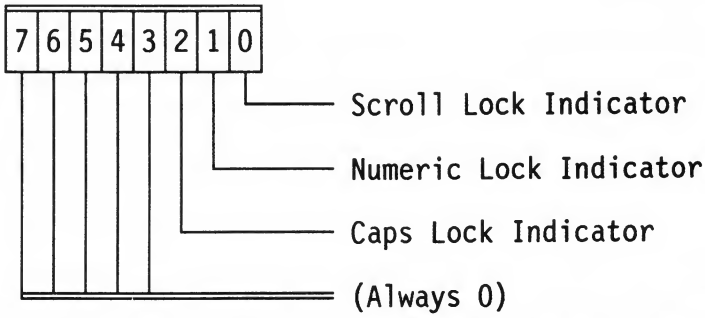
Bit 5	Bit 6	Delay
0	0	250
0	1	500
1	0	750
1	1	1000

Echo

The keyboard transmits a code "EE" response and continues scanning (when preceeded as an Enable).

Set/Reset mode indicators
This command is made up of a 2 – byte command and an option. The keyboard responds to the host side with and ACK command and waits for sending of the option. Then keyboard responds to the option, sets the indicator and starts scanning (when proceeded as an Enable). If it receives another command instead of the option, the indicator condition remains unchanged and the keyboard stops, this command operation. Then proceeds the new command and starts scanning.

TABLE 2 – 33. OPTION REGISTER FOR KEYBOARD



Read Keyboard ID
The keyboard responds with the ACK command, transmits a 2 – byte data ; "AB" + "83"

Set/Read key code mode
This command is made up of a 2 – byte command an option. The keyboard responds to the host side with an ACK command stops scanning and waits for the option. When keyboard inputs option, it responds to the host side with an ACK command, starts scanning after setting key code mode or transmission status. (When proceeded as an Enable.) If it receives another command instead of the option, processing of this command is cancelled, the new command is proceeded and scanning starts.

Read key code mode starts (option data "00"). The keyboard transmits the current keycode mode status. (1 byte)

TABLE 2 – 34. KEY CODE MODE STATUS

KEY CODE MODE	TRANSMITTING DATA
(a)	01
(b)	02
(c)	03

Set key code mode (option data : "01" – "03"). The keyboard is set to specified key code mode depending on the option data.

TABLE 2-35. KEY CODE MODE ON OPTION DATA

Option Data	*Key Code Mode*
01	(a)
02	(b)
03	(c)

Typematic key set
This command is made up of a command and an option (Max 4 or 5 bytes). The keyboard responds to this command with an ACK command, stops scanning and responds to the option with an ACK command. In the key code mode (c), this command sets the typematic function and cancels break code transmission for keys waiting for the key scan codes that correspond to the option data. When the command has been proceeded, scanning stops and remains in that condition.

Typematic key reset 1 ("FC")
This command releases the typematic function and sets transmission of the break code for keys waiting for key scan codes corresponding to option data. Other details are the same as described in the case of typematic key set above.

Typematic key reset 2 ("FD")
This command releases the typematic function and cancels transmission of the break code for keys waiting for key scan codes corresponding to the option data. Other details are the same as described in the case of Typematic key set above.

All key typematic control
The keyboard responds to this command with an ACK command cancels or sets the typematic function and break code transmission and continues scanning (when proceeded as an Enable.)

TABLE 2-36. ALL KEY TYPEMATIC CONTROL

Command Data	Typematic Function	Break Code Transmission	Remarks
FA	Setting	Setting	Applies only to key code mode (c).
F9	Cancel	Cancel	
F8	Cancel	Setting	
F7	Setting	Cancel	

2.5.8.2 COMMANDS TO HOST SIDE

These are commands transmitted to the host side by the keyboard.

TABLE 2-37. COMMANDS TO THE HOST SIDE

COMMAND	DATA (HEX)
Resend	FE
ACK	FA
Overrun	**
Break Code Prefix	F0
BAT Completion	AA
Echo Response	EE
Read Keyboard ID	AB + 83
Read Key Code Mode	Mode (a) + 01 Mode (b) + 02 Mode (c) + 03

** = Key Code Mode (a) ..... FF
Key Code Mode (b),(c) .. 00

Resend
The keyboard generates a resend command when it receives an invalid input or invalid parity input.

ACK
The keyboard outputs an ACK response for valid inputs that do not generate echo or resend commands. If an interrupt is issued to the keyboard when an ACK command is being transmitted, transmission is terminated and the new command is responded to.

Break code prefix
This command announces that a key has been released and sends the first byte of a 2-byte message. (Corresponds to key code mode (b) and (c).)

Overrun
The overrun character is in the 17th position of the keyboard buffer and when the buffer becomes full, the character is stacked on the last code. When this code comes first in the buffer it is output as an overrun error.

BAT completion code
When BAT is completed normally, the keyboard outputs an "AA" response. "FC" or other code indicates that the keyboard microprocessor is malfunctioning.

Echo response
This command is transmitted in response to an echo command from the host side.

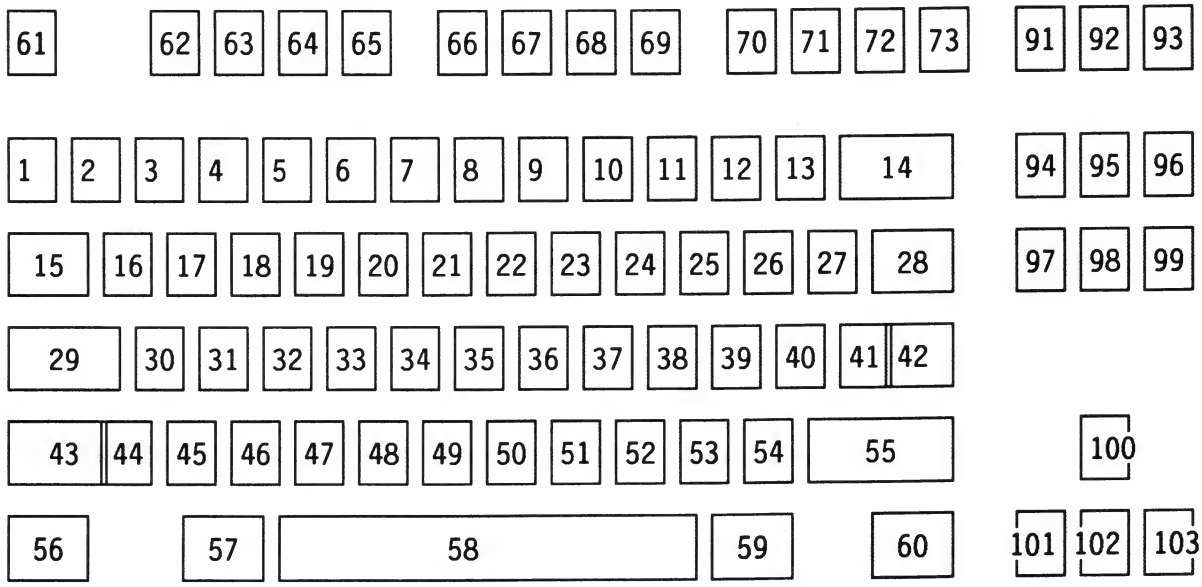
Read keyboard ID
This command is transmitted in response to an equipment ID data read command from the host side.

Read key code mode
This command transmits current keycode mode status in response to a key code mode read command from the host side.

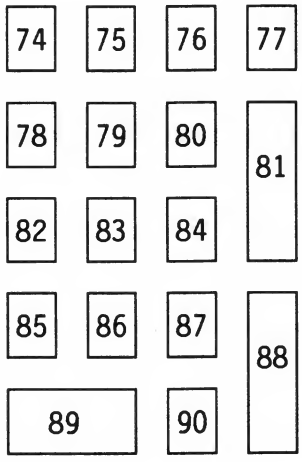
2.5.9 SCAN CODES

The following tables contain the specific scan codes used by the computer. The complete USA layout table is given; the codes for the typewriter area are given first, then the codes for the special function keys, the numeric keypad, and the cursor control keys. (These are followed by tables of differences for the main keyboard in each international layout supported by MS – DOS.)

The scan codes and buffered keycodes are all given in hexadecimal; – – – indicates that the key combination is suppressed in the keyboard routine. The decimal key numbers used in the first column of the table are shown in this diagram:



Numeric keypad keys



(Note: Key number 28 is only present on the US ASCII keyboard, and key numbers 41 and 44 are only present on the other keyboard layouts. Keys 28 and 44 are functionally equivalent, but there is no key corresponding to key number 41 on a US keyboard.)

Character codes and scan codes

US ASCII

Typewriter area

Key Number	Key Marking	Scan Code	Buffered Keycodes			
			Normal	Shift	Ctrl	Alt
1	`	29	60	7E	---	F0+29
2	1	02	31	21	---	00+78
3	2	03	32	40	00+03	00+79
4	3	04	33	23	---	00+7A
5	4	05	34	24	---	00+7B
6	5	06	35	25	---	00+7C
7	6	07	36	5E	1E	00+7D
8	7	08	37	26	---	00+7E
9	8	09	38	2A	---	00+7F
10	9	0A	39	28	---	00+80
11	0	0B	30	29	---	00+81
12	-	0C	2D	5F	1F	00+82
13	=	0D	3D	2B	---	00+83
14	Backspace	0E	08	08	7F	F0+0E
15	Tab	0F	09	00+0F	00+94	00+A5
16	Q	10	71	51	11	00+10
17	W	11	77	57	17	00+11
18	E	12	65	45	05	00+12
19	R	13	72	52	12	00+13
20	T	14	74	54	14	00+14
21	Y	15	79	59	19	00+15
22	U	16	75	55	15	00+16
23	I	17	69	49	09	00+17
24	O	18	6F	4F	0F	00+18
25	P	19	70	50	10	00+19
26	[	1A	5B	7B	1B	F0+1A
27	]	1B	5D	7D	1D	F0+1B
28	\	2B	5C	7C	1C	F0+2B
29	Caps Lock	3A	---	---	---	---
30	A	1E	61	41	01	00+1E
31	S	1F	73	53	13	00+1F
32	D	20	64	44	04	00+20
33	F	21	66	46	06	00+21
34	G	22	67	47	07	00+22
35	H	23	68	48	08	00+23
36	J	24	6A	4A	0A	00+24
37	K	25	6B	4B	0B	00+25
38	L	26	6C	4C	0C	00+26
39	;	27	3B	3A	---	F0+27

40	'	28	27	22	---	F0+28
42	Enter	1C	0D	0D	0A	F0+1C
43	Shift	2A	---	---	---	---
45	Z	2C	7A	5A	1A	00+2C
46	X	2D	78	58	18	00+2D
47	C	2E	63	43	03	00+2E
48	V	2F	76	56	16	00+2F
49	B	30	62	42	02	00+30
50	N	31	6E	4E	0E	00+31
51	M	32	6D	4D	0D	00+32
52	,	33	2C	3C	---	F0+33
53	.	34	2E	3E	---	F0+34
54	/	35	2F	3F	---	F0+35
55	Shift	36	---	---	---	---
56	Ctrl	1D	---	---	---	---
57	Alt	38	---	---	---	---
58	(space)	39	20	20	20	20
59	Alt	E0,38	---	---	---	---
60	Ctrl	E0,1D	---	---	---	---

Special function keys

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
61	Esc	01	1B	1B	1B	F0+01
62	F1	3B	00+3B	00+54	00+5E	00+68
63	F2	3C	00+3C	00+55	00+5F	00+69
64	F3	3D	00+3D	00+56	00+60	00+6A
65	F4	3E	00+3E	00+57	00+61	00+6B
66	F5	3F	00+3F	00+58	00+62	00+6C
67	F6	40	00+40	00+59	00+63	00+6D
68	F7	41	00+41	00+5A	00+64	00+6E
69	F8	42	00+42	00+5B	00+65	00+6F
70	F9	43	00+43	00+5C	00+66	00+70
71	F10	44	00+44	00+5D	00+67	00+71
72	F11	57	00+85	00+87	00+89	00+8B
73	F12	58	00+86	00+88	00+8A	00+8C
91	Prnt Scrn	E0,2A, E0,37	---	---	00+72	---
92	Scrll Lck	46	---	---	---	---
93	Pause	E1,1D, 45,E1, 9D,C5	---	---	00+00	---

Numeric keypad

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Num Lock	Ctrl	Alt
74	Num Lock	45	---	---	---	---
75	/	E0,35	E0+2F	E0+2F	00+95	00+A4
76	*	37	2A	2A	00+96	F0+37
77	-	4A	2D	2D	00+8E	F0+4A
78	7	47	00+47	37	00+77	*
79	8	48	00+48	38	00+8D	*
80	9	49	00+49	39	00+84	*
81	+	4E	2B	2B	00+90	F0+4E
82	4	4B	00+4B	34	00+73	*
83	5	4C	F0+4C	35	00+8F	*
84	6	4D	00+4D	36	00+74	*
85	1	4F	00+4F	31	00+75	*
86	2	50	00+50	32	00+91	*
87	3	51	00+51	33	00+76	*
88	Enter	E0,1C	0D	0D	0A	00+A6
89	0	52	00+52	30	00+92	*
90	.	53	00+53	2E	00+93	---

Cursor control

Key Number	Key Marking	Scan Code	Buffered Keycodes			
			Normal	Shift	Ctrl	Alt
94	Insert	E0,2A, E0,52	E0+52	E0+52	E0+92	00+A2
95	Home	E0,2A, E0,47	E0+47	E0+47	E0+77	00+97
96	Page Up	E0,2A, E0,49	E0+49	E0+49	E0+84	00+99
97	Delete	E0,2A E0,53	E0+53	E0+53	E0+93	00+A3
98	End	E0,2A, E0,4F	E0+4F	E0+4F	E0+75	00+9F
99	Pg Dwn	E0,2A, E0,51	E0+51	E0+51	E0+76	00+A1
100	|	E0,2A, E0,48	E0+48	E0+48	E0+8D	00+98
101	<—	E0,2A, E0,4B	E0+4B	E0+4B	E0+73	00+9B
102	| v	E0,2A, E0,50	E0+50	E0+50	E0+91	00+A0
103	—>	E0,2A, E0,4D	E0+4D	E0+4D	E0+74	00+9D

United Kingdom

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
1	`	29	60	170	---	F0+29
3	2	03	32	22	00+03	00+79
4	3	04	33	9C	---	00+7A
40	'	28	27	40	---	F0+28
41	#	2B	23	7E	1C	F0+2B
44	\	56	5C	7C	---	---

In addition there is one key that produces a different character in the graphics shift mode:

Key Number	Scan Code	Graphics Mode	
		Code	Character
1	29	DD	▌

France

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
1	²	29	FD	---	---	F0+29
2	&	02	26	31	---	00+78
3	é	03	82	32	00+03	00+79
4	"	04	22	33	---	00+7A
5	'	05	27	34	---	00+7B
6	(	06	28	35	---	00+7C
7	-	07	2D	36	1F	00+7D
8	è	08	8A	37	---	00+7E
9	_	09	5F	38	---	00+7F
10	ç	0A	87	39	---	00+80
11	à	0B	85	30	---	00+81
12	)	0C	29	F8	---	00+82
16	A	10	61	41	01	00+1E
17	Z	11	7A	5A	1A	00+2C
26	^	1A	5E*	FE*	1B	F0+1A
27	$	1B	24	9C	1D	F0+1B
30	Q	1E	71	51	11	00+10
39	M	27	6D	4D	0D	00+32
40	ù	28	97	25	---	F0+28
41	*	2B	2A	E6	1C	F0+2B
44	<	56	3C	3E	---	---
45	W	2C	77	57	17	00+11
51	,	32	2C	3F	---	00+27
52	;	33	3B	2E	---	F0+33
53	:	34	3A	2F	---	F0+34
54	!	35	21	15	---	F0+35

* this code is used to begin dead key sequences

In addition there are 12 keys that produce a different character in the graphics shift mode:

Key Number	Scan Code	Graphics Mode	
		Code	Character
3	03	7E	~
4	04	23	#
5	05	7B	{
6	06	5B	[
7	07	7C	|
8	08	60	`

Key Number	Scan Dode	Graphics Mode	
		Code	Character
9	09	5C	\
10	0A	5E	^
11	0B	40	@
12	0C	5D	]
13	0D	7D	}
27	1B	0F	

Germany

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
1	^	29	5E*	F8	---	F0+29
3	2	03	32	22	00+03	00+79
4	3	04	33	15	---	00+7A
7	6	07	36	26	1E	00+7D
8	7	08	37	2F	---	00+7E
9	8	09	38	28	---	00+7F
10	9	0A	39	29	---	00+80
11	0	0B	30	3D	---	00+81
12	ß	0C	E1	3F	---	00+82
13	'	0D	27*	60*	---	00+83
21	Z	15	7A	5A	1A	00+2C
26	Ü	1A	81	9A	1B	F0+1A
27	+	1B	2B	2A	1D	F0+1B
39	Ö	27	94	99	---	F0+27
40	Ä	28	84	8E	---	F0+28
41	#	2B	23	27	1C	F0+2B
44	<	56	3C	3E	---	---
45	Y	2C	79	59	19	00+15
52	,	33	2C	3B	---	F0+33
53	.	34	2E	3A	---	F0+34
54	-	35	2D	5F	---	F0+35

* this code is used to begin dead key sequences

In addition there are 11 keys that produce a different character in the graphics shift mode:

Key Number	Scan Code	Graphics Mode	
		Code	Character
3	03	FD	²
4	04	FC	ⁿ
8	08	7B	{
9	09	5B	[
10	0A	5D	]
11	0B	7D	}

Key Number	Scan Code	Graphics Mode	
		Code	Character
12	0C	5C	\
16	10	40	@
27	1B	7E	~
44	56	7C	¦
51	32	E6	µ

Italy

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
1	\	29	5C	7C	---	F0+29
3	2	03	32	22	00+03	00+79
4	3	04	33	9C	---	00+7A
7	6	07	36	26	1E	00+7D
8	7	08	37	2F	---	00+7E
9	8	09	38	28	---	00+7F
10	9	0A	39	29	---	00+80
11	0	0B	30	3D	---	00+81
12	'	0C	27	3F	---	00+82
13	ì	0D	8D	5E	---	00+83
26	è	1A	8A	82	1B	F0+1A
27	+	1B	2B	2A	1D	F0+1B
39	ò	27	95	87	---	F0+27
40	à	28	85	F8	---	F0+28
41	ù	2B	97	15	1C	F0+2B
44	<	56	3C	3E	---	---
52	,	33	2C	3B	---	F0+33
53	.	34	2E	3A	---	F0+34
54	-	35	2D	5F	---	F0+35

* this code is used to begin dead key sequences

In addition there are four keys that produce a different character in the graphics shift mode:

Key Number	Scan Code	Graphics Mode	
		Code	Character
26	1A	5B	[
27	1B	5D	]
39	27	40	@
40	28	23	#

Spain

Key Number	Key Marking	Scan Code	Buffered Keycode			
			Normal	Shift	Ctrl	Alt
1	º	29	A7	A6	---	F0+29
3	2	03	32	22	00+03	00+79
4	3	04	33	FA	---	00+7A
7	6	07	36	26	1E	00+7D
8	7	08	37	2F	---	00+7E
9	8	09	38	28	---	00+7F
10	9	0A	39	29	---	00+80
11	0	0B	30	3D	---	00+81
12	'	0C	27	3F	---	00+82
13	¡	0D	AD	A8	---	00+83
26		1A	60*	5E*	1B	F0+1A
27	+	1B	2B	2A	1D	F0+1B
39	Ñ	27	A4	A5	---	F0+27
40	'	28	27*	F9*	---	F0+28
41	Ç	2B	87	80	1C	F0+2B
44	<	56	3C	3E	---	---
52	,	33	2C	3B	---	F0+33
53	.	34	2E	3A	---	F0+34
54	-	35	2D	5F	1F	F0+35

* this code is used to begin dead key sequences

In addition there are nine keys that produce a different character in the graphics shift mode:

Key Number	Scan Code	Graphics mode	
		Code	Character
1	29	5C	\
2	02	7C	|
3	03	40	@
4	04	23	#
7	07	AA	¬

Key Number	Scan Code	Graphics Mode	
		Code	Character
26	1A	5B	[
27	1B	5D	]
40	28	7B	{
41	2B	7D	}

2.6 GATE ARRAY DESCRIPTIONS

2.6.1 GAATAB

GAATAB controls the CPU address bus, system address bus and the internal address bus. It has an 8 – bit refresh counter.

GAATAB Pinout Diagram

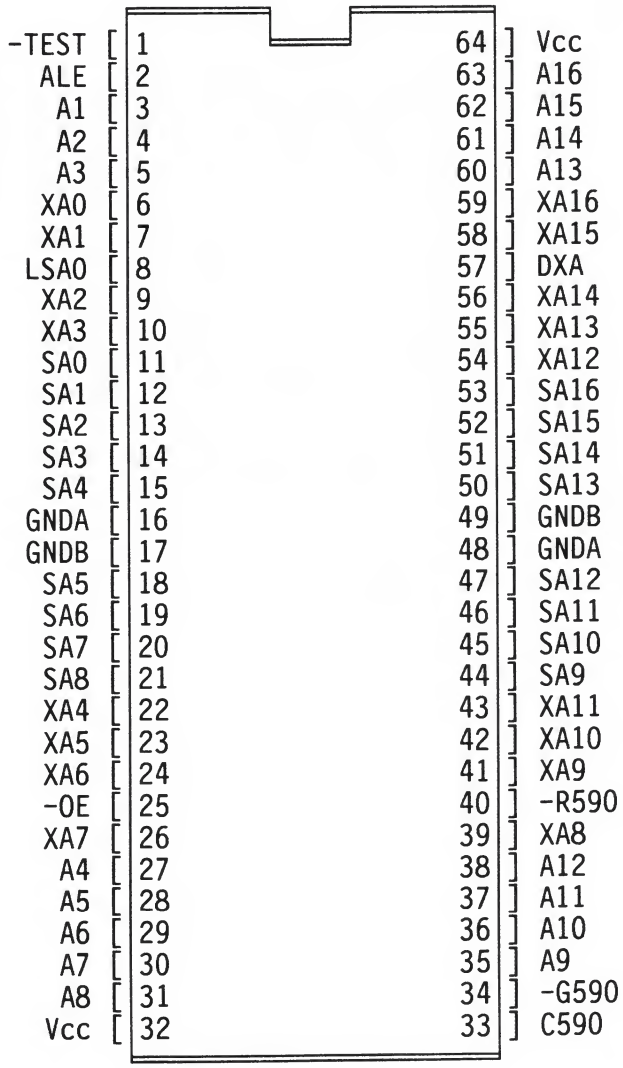


TABLE 2-38. GAATAB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A16-1	I	63-60,38-35, 31-27,5-3	CPU address bus.
LSA0	I	8	Converted address 0. It is identical to CPU address 0 (A0), except during word to byte conversion.
SA16-0	Bus	53-50, 47-44 21-18, 15-11	System address bus.
XA16-0	Bus	59, 58, 56-54, 43-41, 39, 26, 24-22, 10, 9, 7, 6	Internal address bus.
ALE	I	2	Address latch enable. A16-1 are latched by ALE.
-OE	I	25	Enable control of latched address (A16-1). When LOW, LSA0 and latched A16-1 are enabled.
DXA	I	57	Direction control of internal address bus(XA16-0) buffer. When HIGH XA16-0 are driven by SA16-0, and when LOW SA16-0 are driven by XA16-0.
C590	I	33	Clock of refresh counter. Refresh counter increments at C590 rising edge.
-G590	I	34	Output enable of refresh counter. When LOW, refresh address is placed on SA7-0.
-R590	I	40	Reset on refresh counter. When LOW, refresh counter is cleared.
TEST	I	1	Test input. Should be pulled up.

* Legend: I = Input Pin
O = Output Pin
Bus = Input, Output, High-Impedance Pin

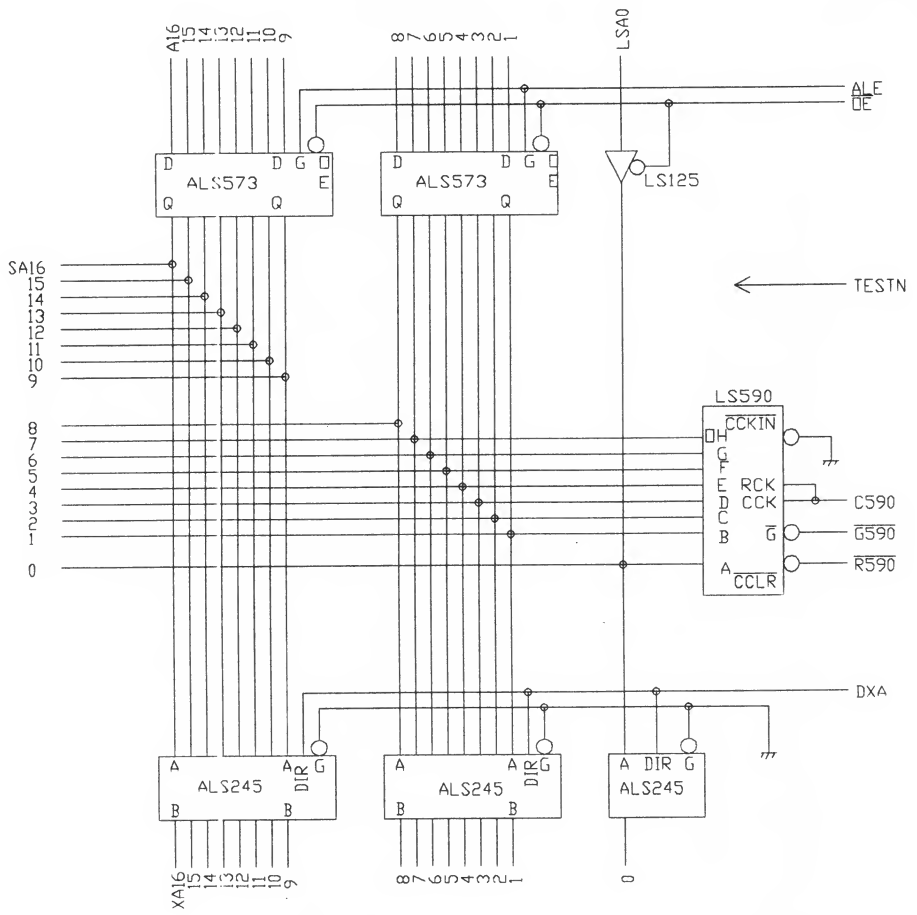
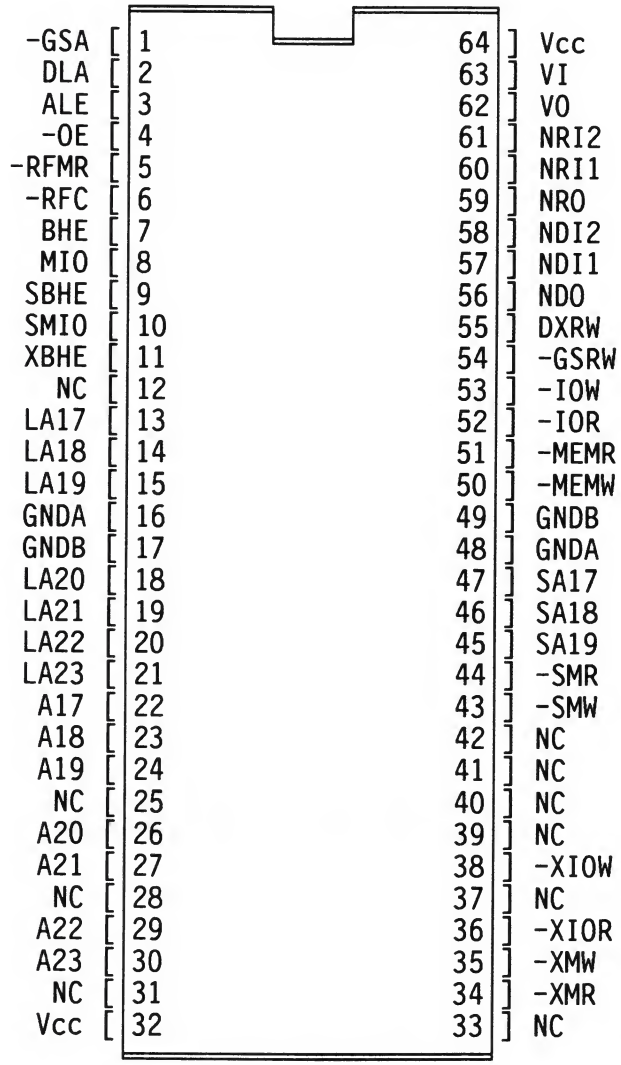


FIGURE 2 – 65. GAATAB INTERNAL BLOCK DIAGRAM

2.6.2 GAATCB

GAATCB controls the CPU control bus and the most significant 7 bits of the address bus. Contains one inverter, one NOR gate and one NAND gate.

GAATCB Pinout Diagram



NC = Not Connected

TABLE 2 – 39. GAATCB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A23 – 17	Bus	30,29,27,26,24 – 22	CPU address bus.
SA19 – 17	Tri	45 – 47	System address bus. (8 – bit connector).
LA23 – 17	Bus	21 – 18, 15 – 13	Unlatched system address bus. (16 – bit connector).
BHE	I	7	CPU bus high enable signal.
SBHE	Bus	9	System bus high enable signal. (16 – bit connector).
XBHE	Bus	11	Internal bus high enable signal.
MIO	I	8	CPU memory / I/O signal.
SMIO	Tri	10	Buffered memory / I/O signal.
– IOW	Bus	53	System I/O write signal. (8 – bit connector).
– IOR	Bus	52	System I/O read signal. (8 – bit connector).
– MEMW	Bus	50	System memory write signal (16 – bit connector).
– MEMR	Bus	51	System memory read signal (16 – bit connector).
– XIOW	Bus	38	Internal I/O write signal.
– XIOR	Bus	36	Internal I/O read signal.
– XMW	Bus	35	Internal memory write signal.
– XMR	Bus	34	Internal memory read signal.
– SMW	Tri	43	System memory write signal (8 – bit connector).
– SMR	Tri	44	System memory read signal (8 – bit connector).
DLA	I	2	Direction control of CPU address bus (A23 – 17) buffer. When HIGH, LA23 – 17 are driven by A23 – 17. When LOW A23 – 17 are driven by LA23 – 17.
– GSA	I	1	Enable control of address bus (SA19 – 17) buffer. When LOW, SA19 – 17 are driven by A19 – 17.
ALE	I	3	Address latch enable. A19 – 17 and MIO and BHE are latched by ALE.
– OE	I	4	Enable control of latched address (A19 – 17), MIO and BHE. When LOW, SA19 – 17 are driven by latched A19 – 17. When LOW, SMIO and SBHE are driven by latched MIO and BHE, respectively.
DXRW	I	55	Direction control of CPU control bus. When HIGH, – XIOW, – XIOR, – XNW and – XNR are driven by – IOW, – IOR, – MEMW, and – MEMR respectively. When LOW, – IOW, – IOR, – MEMW and – MEMR are driven by – XIOW, – XIOR, – XMW, and – XMR respectively.
– GSRW	I	54	Enable control of – SMW and – SMR. When LOW, – SMW and – SMR are enabled.
– RFMR	I	5	Memory read pulse of refresh cycle. – RFMR is used in conjunction with – RFC signal.
– RFC	I	6	Refresh enable. When LOW, – MEMR, – XMR and – SMR are driven by – RFMR.
VI	I	63	Input of inverter.
VO	O	62	Output of inverter.
NDI1	I	57	Input of NAND gate.
NDI2	I	58	Input of NAND gate.
ND0	O	56	Output of NAND gate.
NDI1	I	60	Input of NOR gate.
NDI2	I	61	Input of NOR gate.
NRO	O	59	Output of NOR gate.

* Legend:
I	=	Input Pin
O	=	Ouput Pin
Tri	=	Output / High – impedance Pin
Bus	=	Input / Output / High – impedance Pin

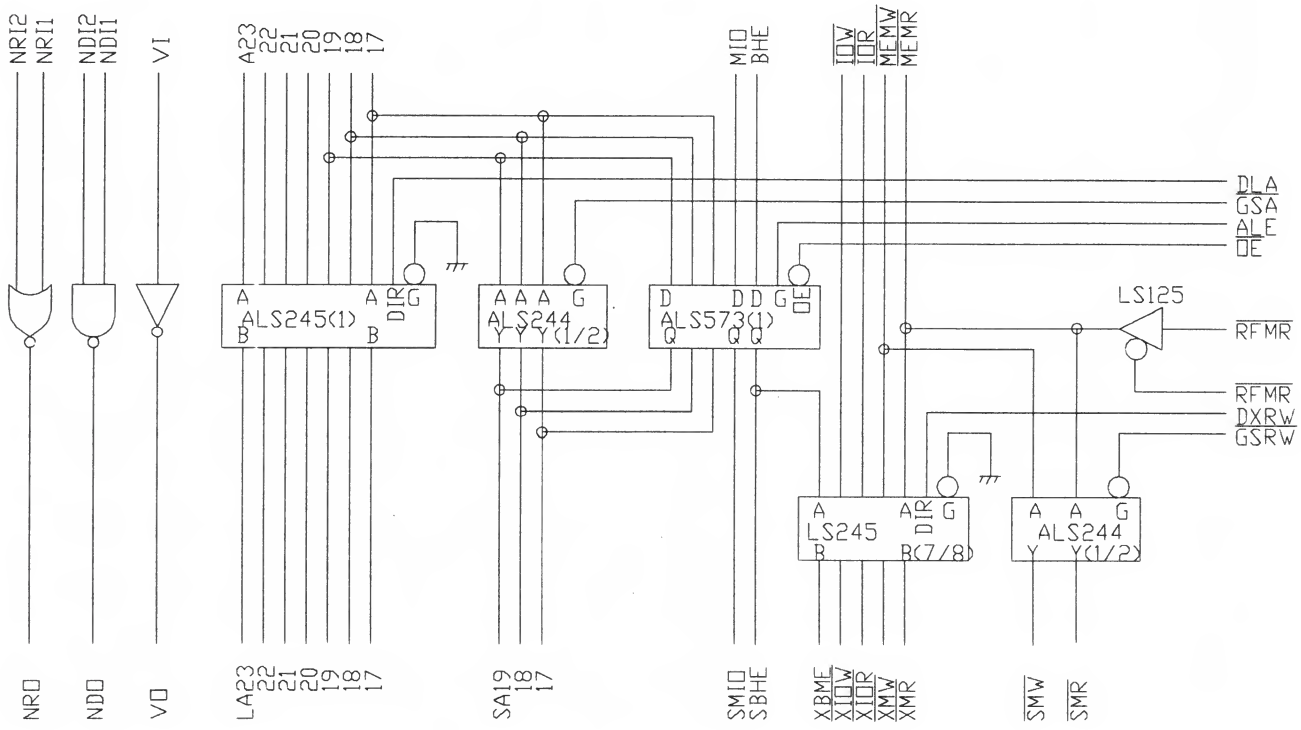
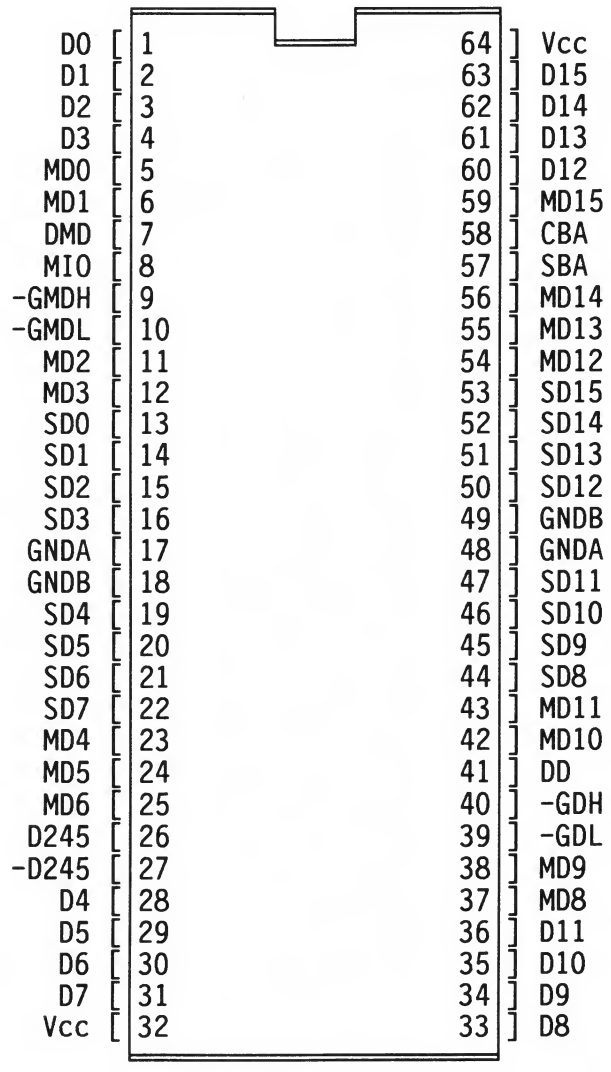


FIGURE 2 – 66. GAATCB INTERNAL BLOCK DIAGRAM

2.6.3 GAATDB

GAATDB has two data bus buffers (system data bus buffer and memory data bus buffer) and a low – to – high byte conversion buffer.

GAATDB Pinout Diagram



NC = Not Connected

TABLE 2-40. GAATDB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
D15-0	Bus	63-60,31-28 4-1,33-36	CPU data bus.
MD15-0	Bus	59,56-54,43, 42,38,37,27, 24,23,22,11, 10,6,5	Memory data bus.
SD15-0	Bus	53-50,47-44 21-18,15-12	System data bus.
DD	I	41	Direction control of CPU data bus (D15-0) buffer. When LOW, CPU reads data from MD15-0 or SD15-0.
-GDH	I	40	Enable control of CPU data bus high byte (D15-8) buffer. When LOW, it enables high byte.
-GDL	I	39	Enable control of CPU data bus low byte (D7-0) buffer. When LOW, it enables low byte.
CBA	I	58	Read data latch. SD7-0 are latched at CBA rising edge.
SBA	I	57	SBA selects latched or un-latched data. When HIGH, latched data are selected. SBA is used in conjunction with CBA signal.
DMD	I	7	Direction control of Memory data bus (MD15-0) buffer. When HIGH Memory data is read.
-GMDH	I	8	Enable control of Memory data high byte (MD15-8) buffer. When LOW, it enables high byte. -GMDH is used in conjunction with DMD signal.
-GMDL	I	9	Enable control of Memory data low byte (MD7-0) buffer. When LOW, it enables low byte. -GMDL is used in conjunction with DMD signal.
D245	I	25	Direction control of low to high byte conversion buffer. When LOW, it indicates high to low byte conversion during data transfers to 8-bit peripherals (write). When HIGH, it indicates low to high byte conversion during data transfers from 8-bit peripherals (read).
-G245	I	26	Enable control of low to high byte conversion buffer. Active LOW signal used in conjunction with D245.

* Legend: I = Input Pin
O = Output Pin
Bus = Input / Output / High-impedance Pin

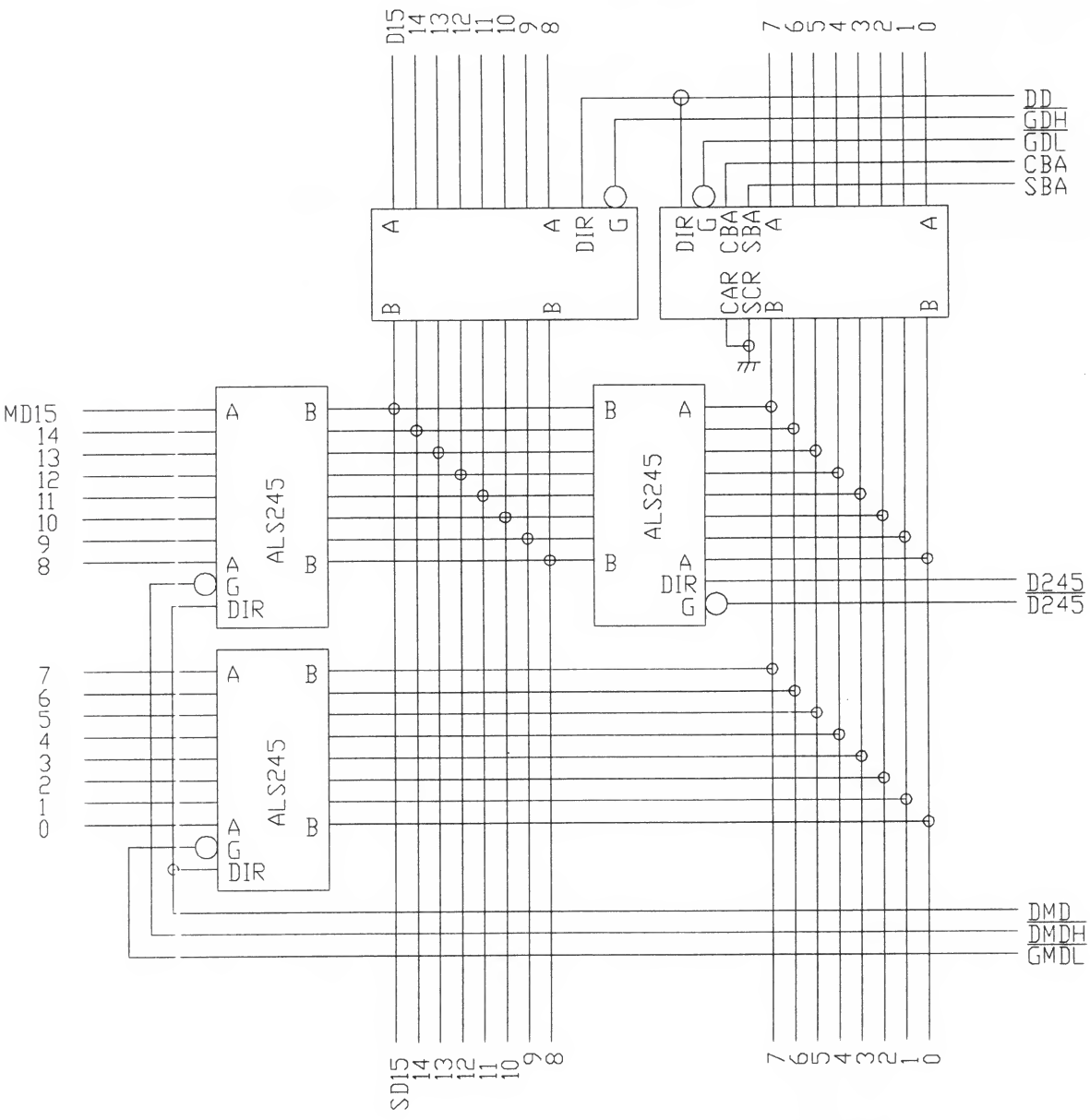


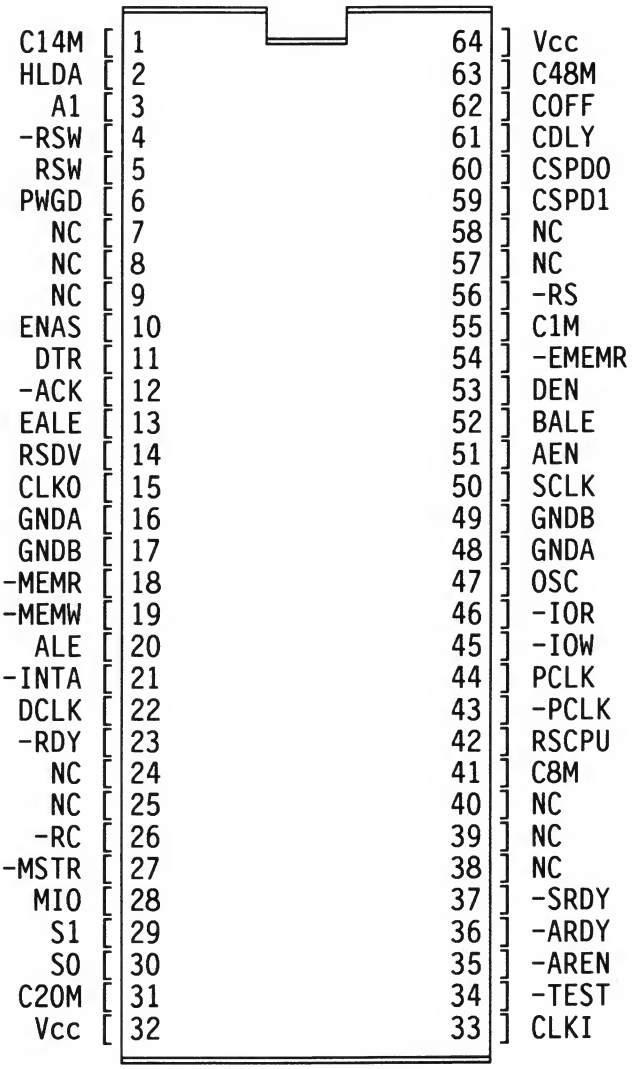
FIGURE 2-67. GAATDB INTERNAL BLOCK DIAGRAM

2.6.4 GAATCK

GAATCK includes following functional blocks.

(1) Clock generator
CPU clock, 80287 clock, System clock,
DMA clock, 8042 clock, 8254 clock,
NTSC clock (14.31818 MHz)
(2) Ready circuit
(3) Reset circuit
(4) Bus controller: – MEMR, – MEMW, – IOR, – IOW, – INTA, ALE, DTR, DEN
(5) Shut down circuit

GAATCK Pinout Diagram



NC = Not Connected

TABLE 2-41. GAATCK PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
C48M	I	63	Clock input. 48 MHz.
C20M	I	31	Clock input. 20 MHz.
C14M	I	1	Clock input. 14.31818 MHz.
PCLK	O	44	KB controller (8042) clock. 6 MHz.
-PCLK	O	43	KB controller (8042) clock. 6 MHz.
OSC	O	47	Clock output. 14.31818 MHz. (for option slot)
C1M	O	55	Clock output. 1.19 MHz. (for 8254)
C8M	O	41	Clock output. 8 MHz, duty 33%. (for 80287)
DCLK	O	22	DMA CLOCK
SCLK	O	50	System clock.
CLKO	O	15	CPU clock output.
CLKI	I	33	CPU clock input. CLKI should be connected to CLKO externally.
CSPD1	I	59	CPU clock select.
CSPD0	I	60	CPU clock select.

CSPD1	*CSPD0*	*SCLK*	*CLKO*	*CLKI*	*DCLK*
0	1	6 MHz	12 MHz	12 MHz	3 MHz
1	1	8 MHz	16 MHz	16 MHz	4 MHz
1	0	10 MHz	20 MHz	20 MHz	5 MHz
0	0	12 MHz	24 MHz	24 MHz	6 MHz

PWGD	I	6	Power good. When LOW, it indidates that power is not good and reset signals (-RS, RSDV, RSCPU) are activated.
-RSW	I	4	Reset switch activation signal. -RSW becomes LOW.
RSWP	I	5	Reset switch activation signal. RSWP becomes LOW.
-RS	O	56	Reset signal. (for internal circuit)
RSDV	O	14	Reset signal. (for option slot)
-AREN	I	35	Asynchronous ready and synchronous ready enable.
-ARDY	I	36	Asynchronous ready input. It is used in conjunction with -AREN.
-SRDY	I	37	Synchronous ready input. It is used in conjunction with -AREN.
-RDY	O	23	Ready output.
MIO	I	28	Memory or I/O select. When LOW, the current bus cycle is in the I/O space.
S1	I	29	Bus cycle status.
S0	I	30	Bus cycle status.

MIO	*S1*	*S0*	*Type of bus cycle*
0	0	0	INTA
0	0	1	IO READ
0	1	0	IO WRITE
0	1	1	NONE, IDLE
1	0	0	HALT OR SHUT DOWN
1	0	1	MEMORY READ
1	1	0	MEMORY WRITE
1	1	1	NONE, IDLE

TABLE 2-41. (Continued)

COFF	I	62	Control off. When HIGH, command and DEN are forced inactive.
CDLY	I	61	Command delay. When HIGH, the start of command output is delayed.
HLDA	I	2	Hold acknowledge. When HIGH, command output becomes 3-state off.
ALE	O	20	Address latch enable.
DEN	O	53	Data bus enable.
DTR	O	11	Data transmit/receive. When HIGH, this control output indicates that a write bus cycle is being performed.
-MEMR	Tri	18	Memory read command.
-MEMW	Tri	19	Memory write command.
-IOR	Tri	46	I/O read command.
-IOW	Tri	45	I/O write command.
-INTA	Tri	21	Interrrupt acknowledge.
-EMEMR	O	54	Early memory read signal.
EALE	O	13	Early address latch enable.
BALE	O	52	Buffered address latch enable.
-MSTR	I	27	Master. A processor or DMA controller on the I/O channel may pull this signal LOW.
-ACK	O	12	Acknowledge. When LOW, DMA controller (or refresh controller) has control of the address bus, data bus and control bus.
AEN	O	51	Address enable.
A1	I	3	Address 1.
-RC	I	26	Reset CPU input from 8042.
RSCPU	O	42	Reset CPU output. When HIGH, CPU is reset. RSCPU becomes active when: (1) PWGD is LOW. (2) Reset switch is activated. (3) 8042 pulls RC signal LOW. (4) CPU executes shutdown cycle.
-ENAS	O	10	Enable control of RTCAS (RTC address strobe) signal.
-TEST	I	34	Test input. TEST should be pulled HIGH.

* Legend: O = Output
I = Input
Tri = Output / High-impedance Pin

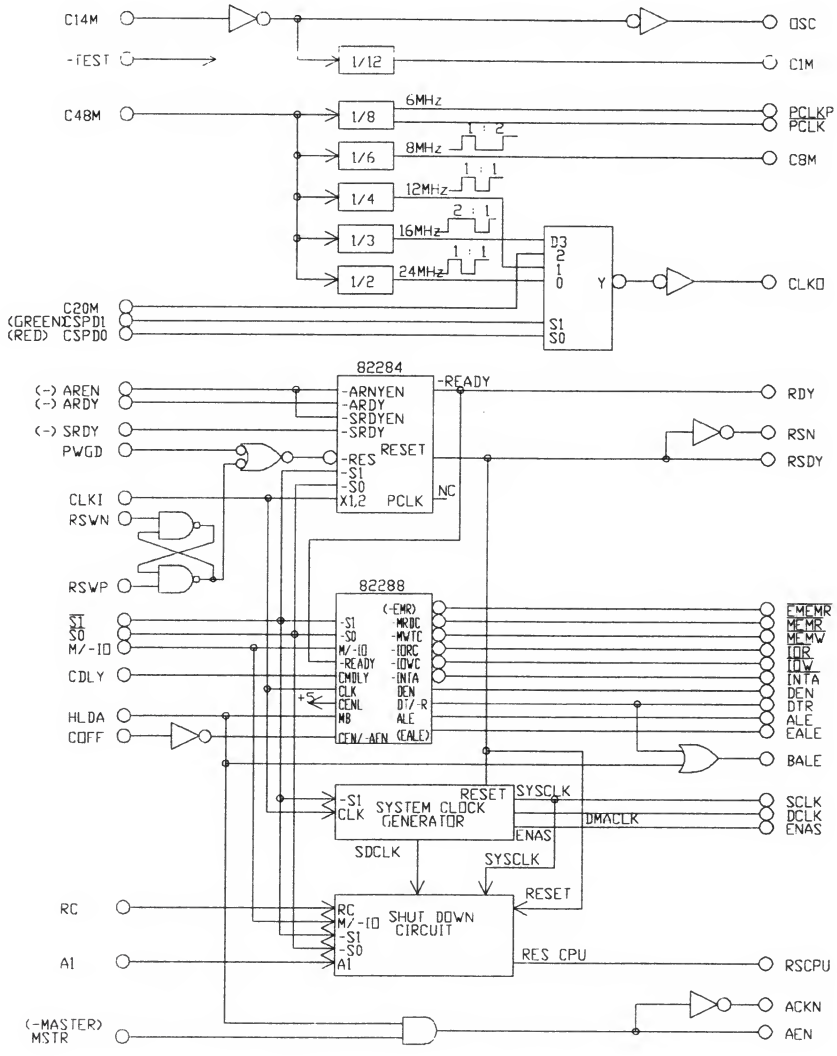


FIGURE 2-68. GAATCK INTERNAL BLOCK DIAGRAM - I

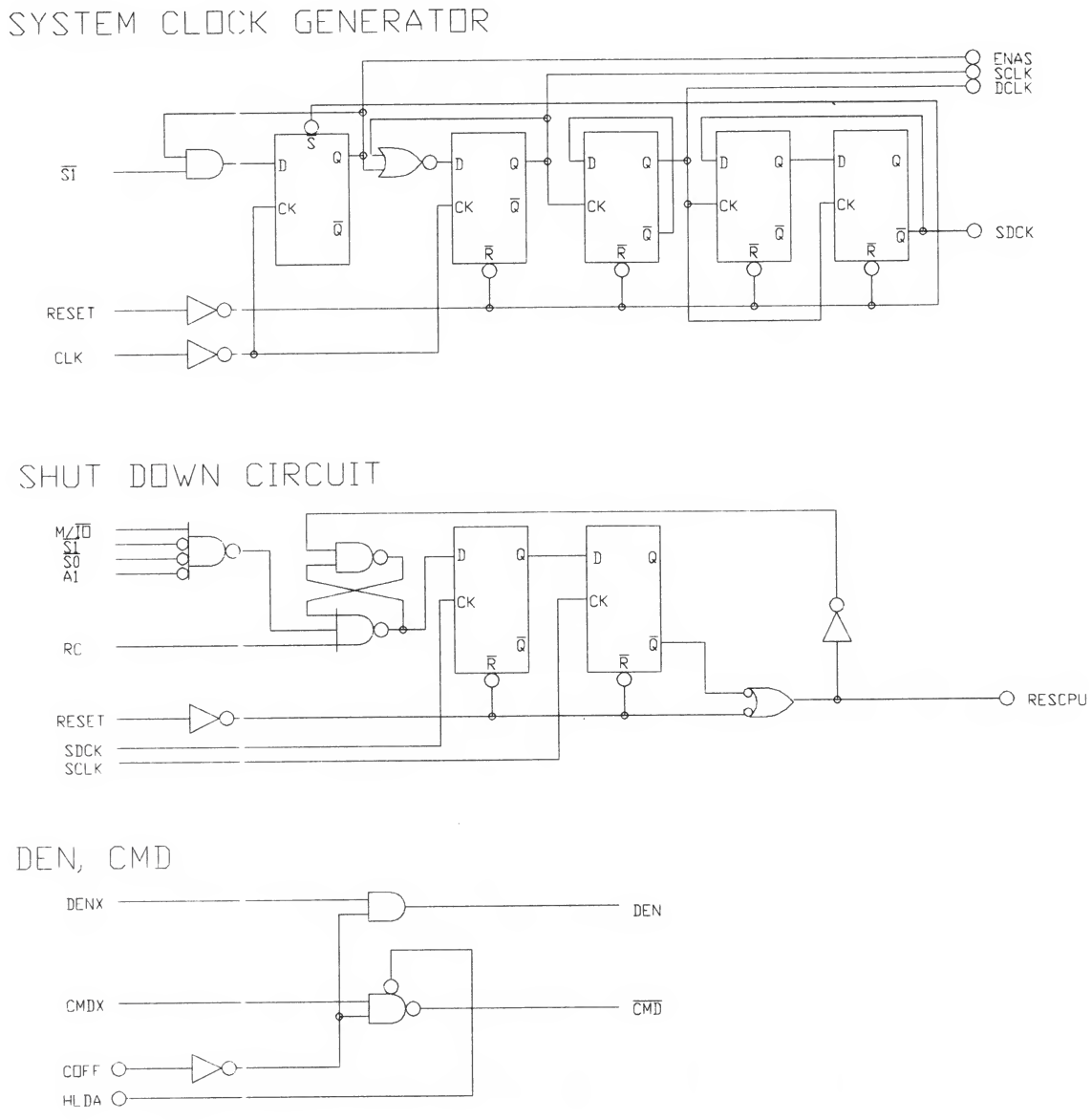


FIGURE 2-69. GAATCK INTERNAL BLOCK DIAGRAM – II

2.6.5 GAATM2

GAATM2 generates memory address and RAS, CAS, WE signals used with GAATM1 and the delay line to control DRAM.

GAATM2 Pinout Diagram

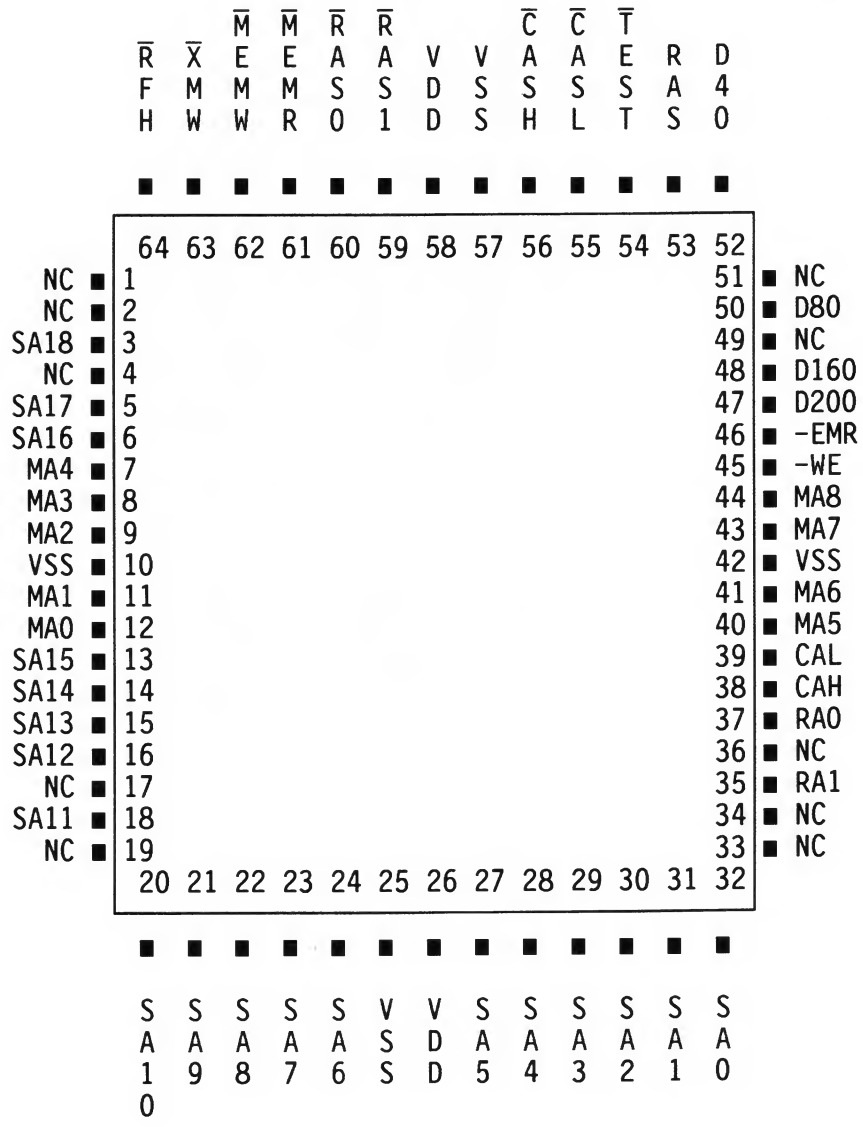


TABLE 2-42. GAATM2 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
SA18-0	I	3,5,6,13-16, 18,20-24, 27-32	System address bus.
MA8-0	O	44,43,41,40, 9-7,12,11	DRAM address bus.
-MEMR	I	61	System memory read signal.
-MEMW	I	62	System memory write signal.
-EMR	I	46	Early memory read signal.
-XMW	I	63	Internal memory write signal.
-RFH	I	64	Refresh signal.
D40	I	52	40 ns delayed signal from RAS.
D80	I	50	80 ns delayed signal from RAS.
D160	I	48	160 ns delayed signal from RAS.
D200	I	47	200 ns delayed signal from RAS.
RA1	I	35	RA1 signal is used to generate RAS1 signal.
RA0	I	37	RA0 signal is used to generate RAS0 signal.
CAH	I	38	CAH signal is used to generate CASH signal.
CAL	I	39	CAL signal is used to generate CASL signal.
-RAS1	O	59	Row address strobe for DRAM (80000H-9FFFFH).
-RAS0	O	60	Row address strobe for DRAM (0H-7FFFFH)
-CASH	O	56	Column address strobe for DRAM (0H-9FFFFH, odd bytes).
-CASL	O	55	Column address strobe for DRAM (0H-9FFFFH, even bytes).
-WE	O	45	Write enable signal for DRAM.
RAS	O	53	RAS is generated from logical OR of MEMR and MEMW. This output is used to generate delay signals (D40, D80, D160, D200)
-TEST	I	54	Test input. TEST should be pulled up.

* Legend: I = Input Pin
O = Ouput Pin

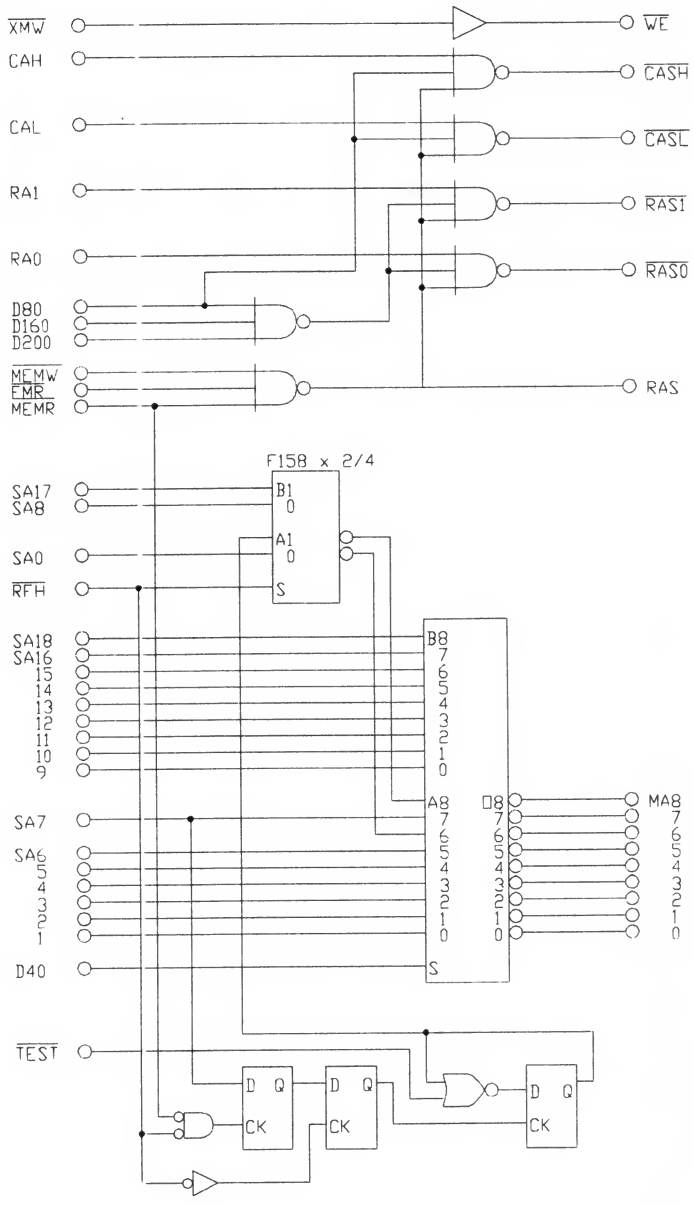


FIGURE 2 – 70. GAATM2 INTERNAL BLOCK DIAGRAM

2.6.6 GAATIO

GAATIO includes following functional blocks.

(1) Address decoder of I/O space.
(2) DMA page register (74LS612 compatible)
(3) Port B.
(4) NMI enable register.
(5) Address latch for DMA.
(6) Interface circuit between NP (80287) and CPU (80286).
(7) General purpose gates.
1 inverter, 1 NAND gate, two 3 – state buffers.

GAATIO Pinout Diagram

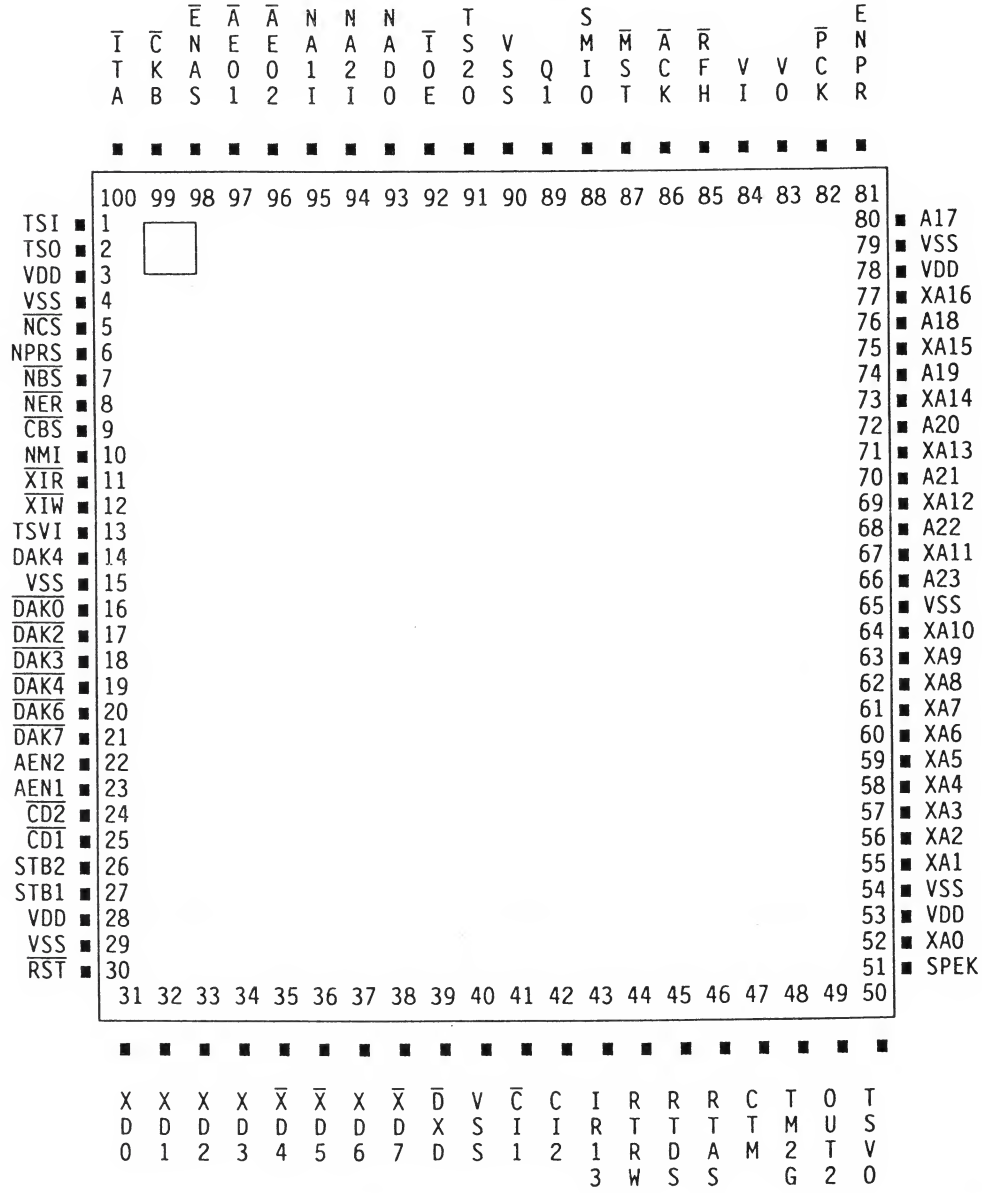


TABLE 2-43. GAATIO PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
XD7-0	Bus	38-3	1Internal data bus.
A23-17	Tri	66,68,70,72, 74,76,80	CPU address bus.
XA16-10	Tri	77,75,73,71, 69,67,64	> >
XA9-8	Bus	62,63	> Internal address bus.
XA7-1	I	61-55	>
XA0	I	52	>
-XIW	I	12	Internal I/O write signal. (= -XIOW)
-XIR	I	11	Internal I/O read signal. (= -XIOR)
-RST	I	30	Reset.
-DK7	I	21	-DACK7. DMA acknowledge 7.
-DK6	I	20	-DACK6. DMA acknowledge 6.
-DK4	I	19	-DACK4. DMA acknowledge 4.
-DK3	I	18	-DACK3, DMA acknowledge 3.
-DK2	I	17	-DACK2. DMA acknowledge 2.
-DK0	I	16	-DACK0. DMA acknowledge 0.
-DAK4	O	14	+DACK4. This signal is output.
-RFH	I	85	Refresh signal.
-ACK	I	86	DMA acknowledge. -ACK is active when DMA or refresh cycle is being performed.
STB2	I	26	DMAC-2 (16-bit DMA controller) address strobe signal.
STB1	I	27	DMAC-1 (8-bit DMA controller) address strobe signal.
AEN2	I	22	Address enable signal of DMAC-2.
AEN1	I	23	Address enable signal of DMAC-1.
-AE02	O	96	AE02 is active when DMAC-2 has control of the system.
-AE01	O	97	AE01 is active when DMAC-1 has control of the system.
MSTN	I	87	-MASTER. When LOW, it indicates that the master on the option slot (DMAC or CPU on the slot) has the control of the system.
ITAN	I	100	-INTA. Interrupt acknowledge.
SMIO	I	88	Memory or I/O select.
-NER	I	8	NP (80287) error.
-NBS	I	7	NP (80287) busy.
Q1	I	89	Timing signal to generate RTAS signal.
-ENAS	I	98	Enable control of RTAS signal.
-CD2	O	24	Chip select of DMAC2 (8237).
-CD1	O	25	Chip select of DMAC1 (8237).
-CI2	O	42	Chip select of INTC2 (8259).
-CI1	O	41	Chip select of INTC1 (8259).
-CTM	O	47	Chip select of system TIMER (8254).
-CKB	O	99	Chip select of keyboard controller (8042).
-RTRW	O	44	Write signal of real time clock (HD146818).
-RTDS	O	45	Read signal of RTC (HD146818)
RTAS	O	46	ALE signal of RTC (HD146818).
NPRS	O	6	NP (80287) reset signal.
-NCS	O	5	Chip select NP (80287).

TABLE 2-43. (Continued)

-CBS	O	9	CPU (80286) busy signal.
IR13	O	43	Interrupt request 13.
DXD	O	39	Direction control of 8 bit internal data bus (XD7-0) buffer.
NMI	O	10	Non-maskable interrupt request.
SPEK	O	51	Output signal for speaker.
TM2G	O	48	Timer CH2 gate. This signal is connected to channel 2 gate input of timer LSI (8254).
ENPR	O	81	Enable RAM parity check.
IOEN	O	92	I/O channel error (option slot).
OUT2	I	49	Timer CH2 output. This signal is connected to channel 2 output of timer LSI (8254).
-PCK	I	82	Parity check error.
VI	I	84	Input of inverter.
VO	O	83	Output of inverter.
NA1I	I	95	Input of NAND gate.
NA2I	I	94	Input of NAND gate.
NADO	O	93	Output of NAND gate.
TS2O	Tri	91	Output of 3-state buffer.
TSI	I	1	Enable control (active LOW) of 3-state buffer.
TSO	Tri	2	Output of 3-state buffer.
TSVI	I	13	Enable control (active LOW) of 3-state buffer.
TSVO	Tri	50	Output of 3-state buffer.

* Legend:
I = Input Pin
O = Ouput Pin
Tri = Output / High-Impedance Pin
Bus = Input / Output / High-Impedance Pin

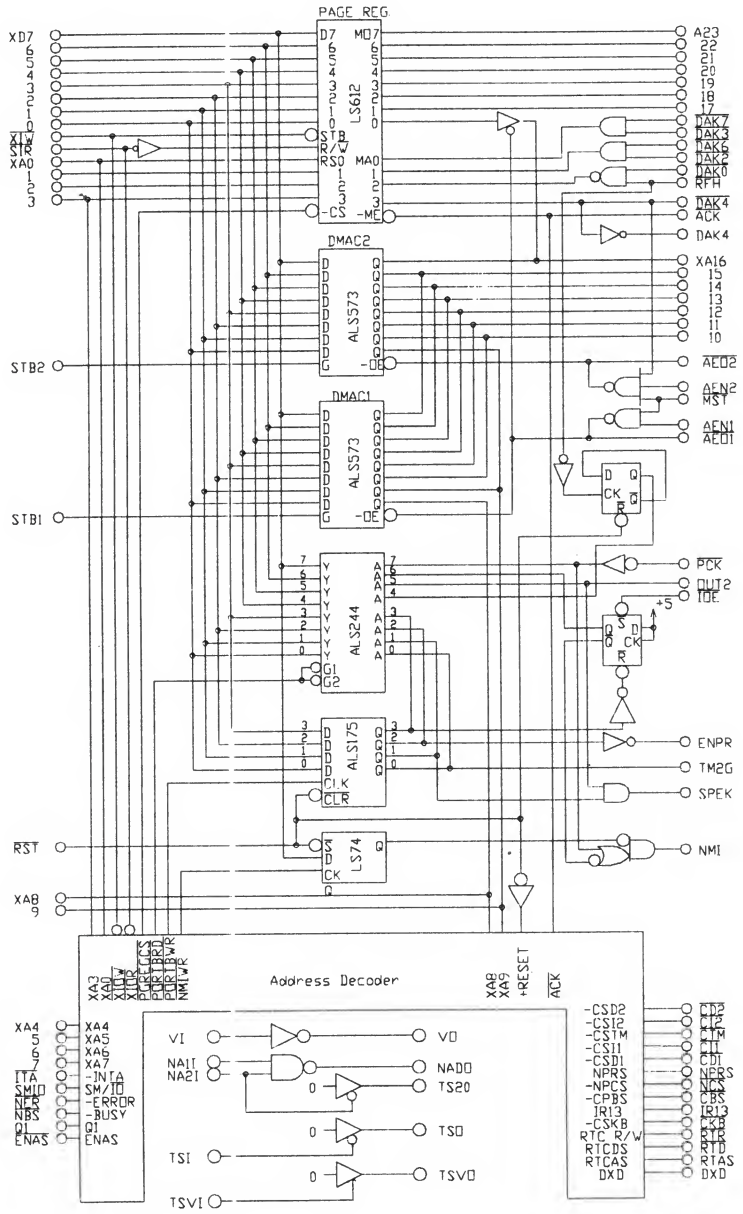


FIGURE 2-71. GAATIO INTERNAL BLOCK DIAGRAM - I

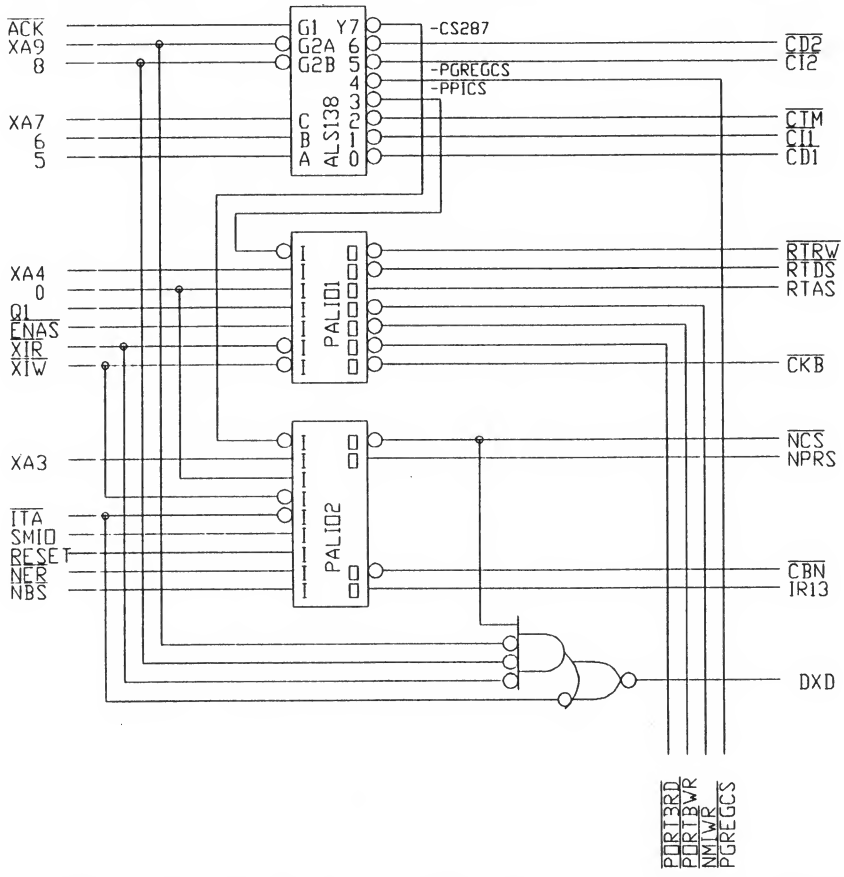


FIGURE 2 – 72. GAATIO INTERNAL BLOCK DIAGRAM – II

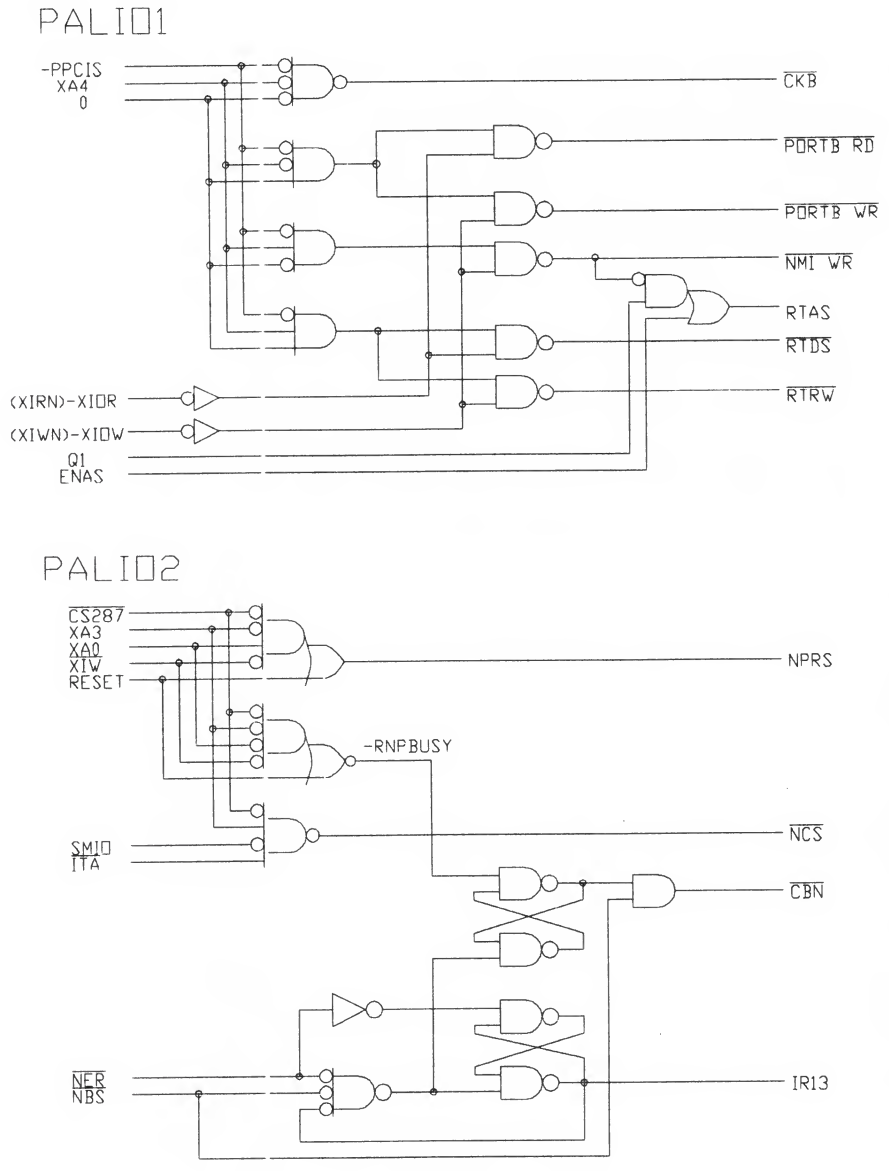


FIGURE 2-73. GAATIO INTERNAL BLOCK DIAGRAM - III

2.6.7 GAATM1

GAATM1 includes the following functional blocks.

1. Address decoder for ROM and DRAM
2. Parity checker / generator
3. Additional circuitry for the memory expansion card

GAATM1 Pinout Diagram

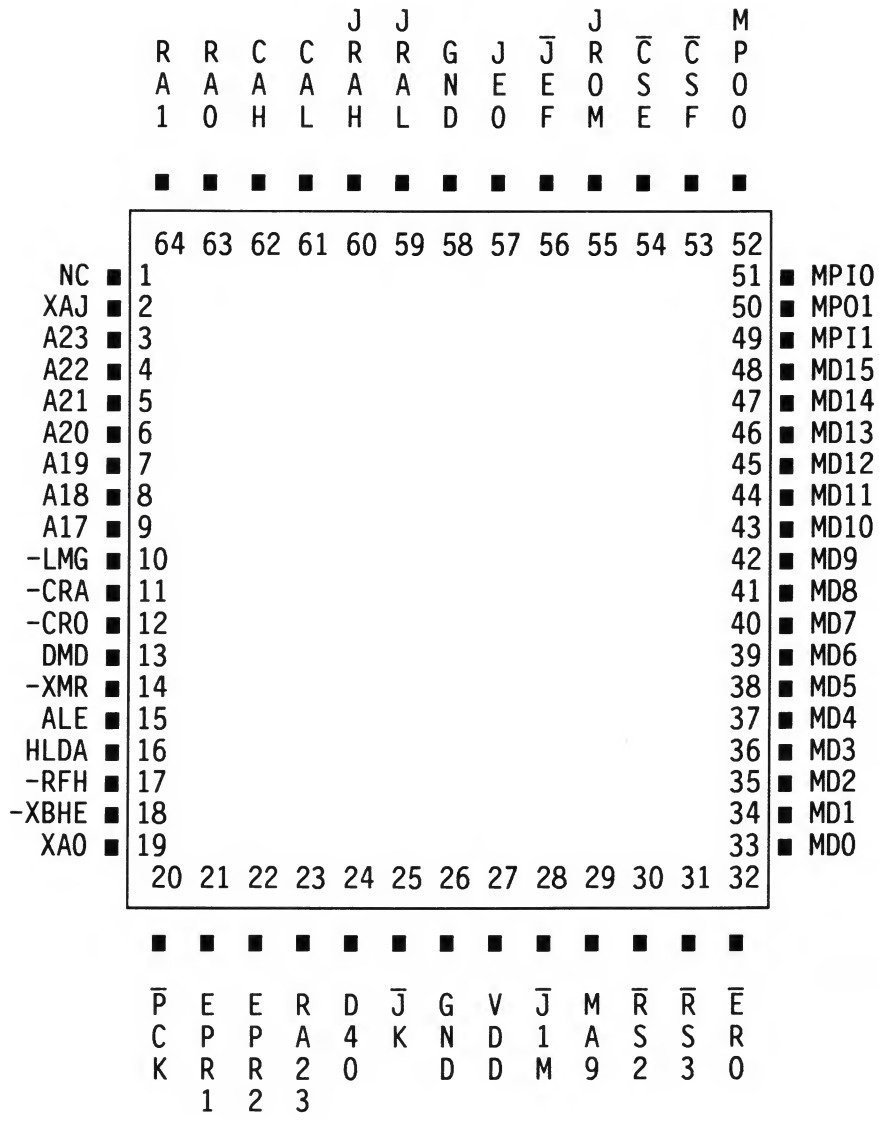


TABLE 2-44. GAATM1 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A23-17	I	3-9	CPU address bus.
-RFH	I	17	Refresh signal.
XAJ	I	2	ROM address select. XA16 or XA15 should be connected to XAJ. ROM address range:

	-CSF	-CSE
XAJ = XA16	0F0000-0FFFFF FF0000-FFFFFF	0E0000-0EFFFF FE0000-FEFFFF
XAJ = XA15	0F8000-0FFFFF FF8000-FFFFFF (0E8000-0EFFFF) (FE8000-FEFFFF)	0F0000-0F7FFF FF0000-FF7FFF (0E0000-0E7FFF) (FE0000-FE7FFF)

ALE	I	15	Address latch enable.
HLDA	I	16	Hold acknowledge.
-XMR	I	14	Internal memory read signal.
XBHE	I	18	Internal bus high enable signal.
XA0	I	19	Internal address bus 0.
JRAH	I	60	Enable control of RAM from 080000H to 09FFFFH.
JRAL	I	59	Enable control of RAM from 040000H to 07FFFFH.
-JEF	I	56	RAM address select. When LOW, RAM address is assigned from F00000H to F9FFFFH. This input should be HIGH or open in EQUITY II+ / EPSON PC AX2.
JE0	I	57	RAM address select. When HIGH, RAM address is assigned from 000000H to 09FFFFH. This input should be HIGH or open in EQUITY II+ / EPSON PC AX2.
JROM	I	55	Enable control of ROM. When HIGH, ROM is enabled. This input should be HIGH or open in EQUITY II+ / EPSON PC AX2.
-J1M	I	28	Chip select input for memory expansion card which uses 1Mbit RAM chips. This input should be HIGH or open in EQUITY II+ / EPSON PC AX2.
-JK	I	25	Chip select input for memory expansion card which uses 256Kbit RAM chips. This signal should be HIGH or open in EQUITY II+ / EPSON PC AX2.
RA23	I	23	Timing input for -RS3 and -RS2. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY II+ / EPSON PC AX2, and should be HIGH or open.
D40	I	24	40ns delayed signal from RAS. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY II+ / EPSON PC AX2, and should be HIGH or open.
-LMG	O	10	Chip select of LOW order 1Mbyte memory space. -LMG is active when memory space from 000000H to 0FFFFFH is accessed.
-CRO	O	12	ROM chip select.

TABLE 2-44. (Continued)

-CRA	O	11	RAM chip select.
-CSF	O	53	Read signal of BIOS ROM.
-CSE	O	54	Read signal of reserved ROM.
RA1	O	64	RA1 signal is used to generate RAS1 signal in GAATM2.
RA0	O	63	RA0 signal is used to generate RAS0 signal in GAATM2.
CAH	O	62	CAH signal is used to generate CASH signal in GAATM2.
CAL	O	61	CAL signal is used to generate CASL signal in GAATM2.
-RS3	O	31	Row address strobe for DRAM. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY II+ / EPSON PC AX2.
-RS2	O	30	(-RAS2) Row address strobe for DRAM. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY II+ / EPSON PC AX2.
DMD	O	13	Direction control of memory data bus buffer.
MA9	O	29	Dynamic RAM address 9. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY II+ / EPSON PC AX2.
DM15-0	I	48-33	Memory data bus.
MP01	I	50	Parity bit of odd address byte. MP01 is parity-checked with MD15-8 in memory read cycle.
MPO0	I	52	Parity bit of even address byte. MPO0 is parity-checked with MD7-0 in memory read cycle.
MPI1	O	49	Parity bit of odd address byte. MPI1 is generated from MD15-8 in memory write cycle.
MPI0	O	51	Parity bit of even address byte. MPI0 is generated from MD7-0 in memory write cycle.
EPR1	I	21	Enable RAM parity check. When HIGH, parity check circuit is enabled. And when LOW, parity check circuit is cleared.
-EPR2	I	22	Enable RAM parity check. This signal Is not used in EQUITY II+ / EPSON PC AX2, and should be pulled down.
-PCK	O	20	Parity error signal. When LOW, it indicates that parity error has occurred.
-ERO	Tri	32	Parity error signal. 3-state output. This signal is not used in EQUITY II+ / EPSON PC AX2.

* Legend: I = Input Pin
O = Output Pin
Tri = Output & High-impedance Pin

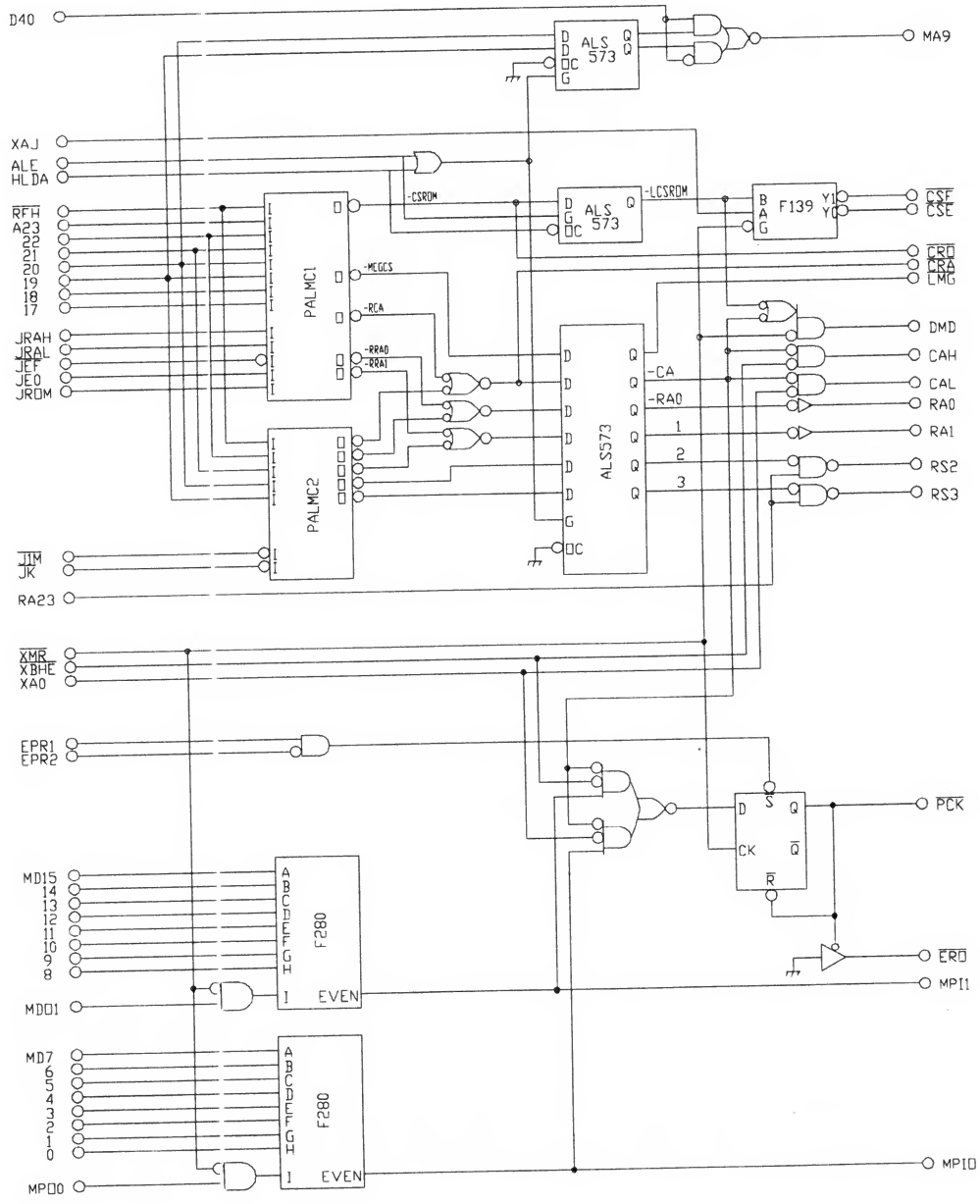


FIGURE 2-74. GAATM1 INTERNAL BLOCK DIAGRAM - I

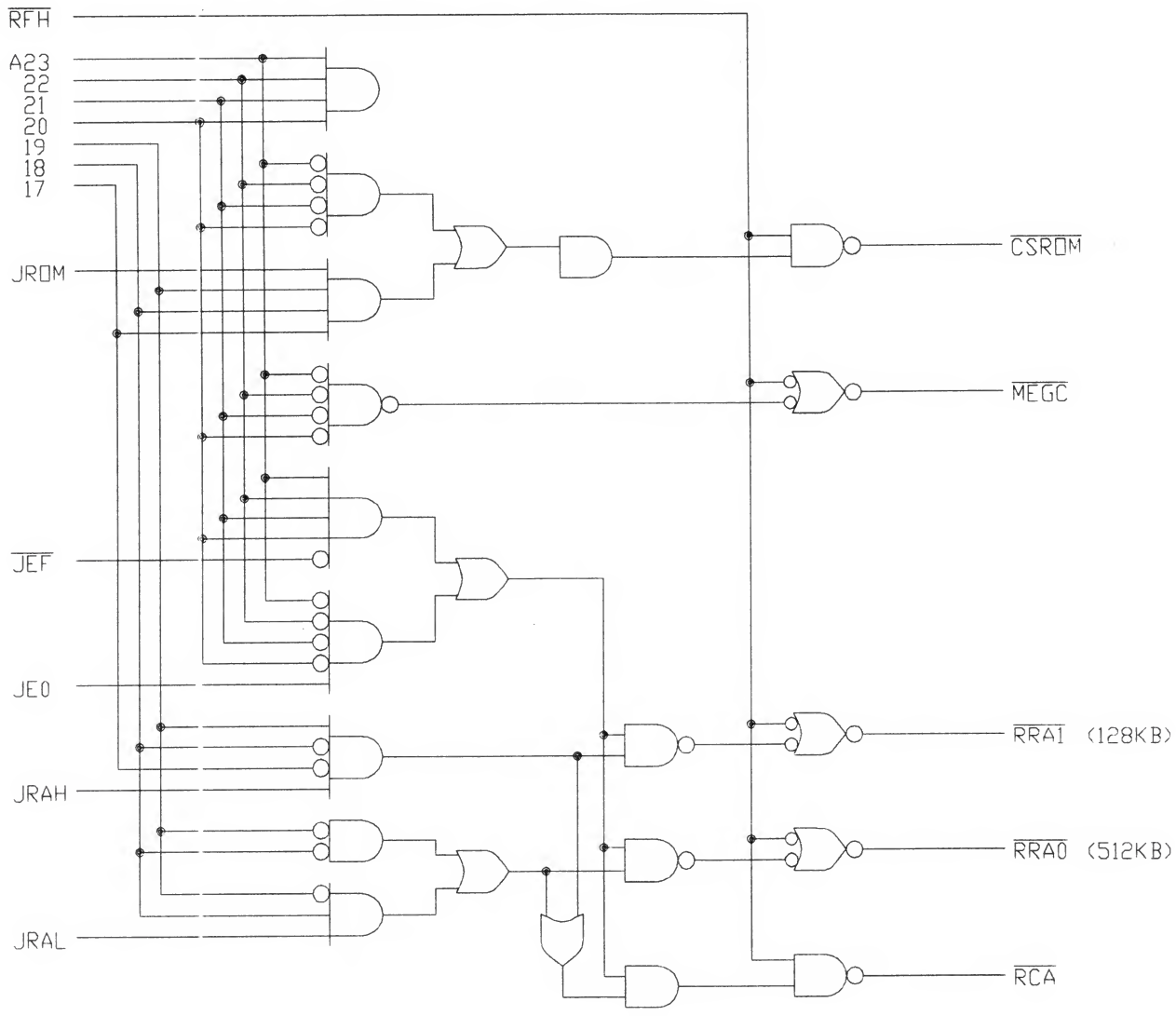


FIGURE 2-75. GAATM1 INTERNAL BLOCK DIAGRAM - II

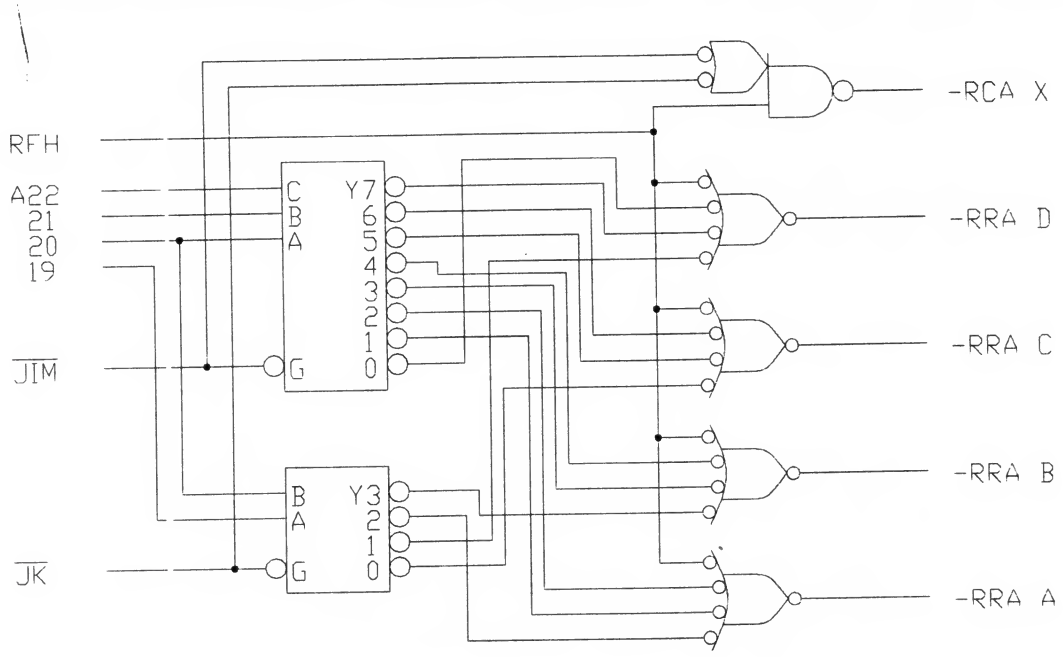


FIGURE 2 – 76. GAATM1 INTERNAL BLOCK DIAGRAM – III

2.6.8 GAATRF

GAATRF includes the following functional blocks.

1. DRAM refresh control circuit.
2. DMA control circuit.
3. 16 < – – > 8 data conversion circuit.
4. Wait states insertion circuit.
5. Command delay control circuit.
6. XA0, XBHE control circuit.

GAATRF Pinout Diagram

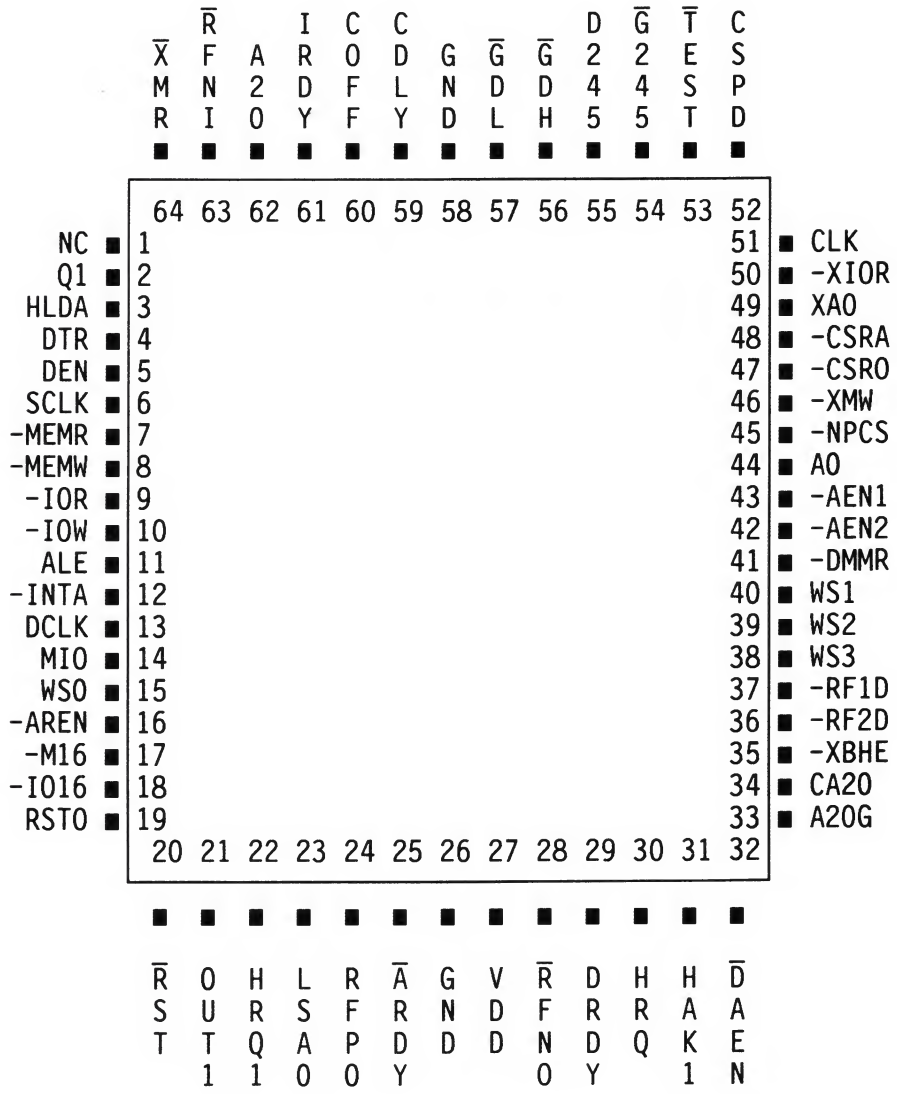


TABLE 2-45. GAATRF PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
WS0	I	15	Zero wait insertion. When LOW, wait state is not inserted. -WS0 signal of option slot is connected to this pin.
WS1	I	40	Wait states control of BIOS ROM access. The number of wait states of BIOS ROM (0E0000-0FFFFF, FE0000-FFFFFF) is controlled by WS1.

CSPD	*WS1*	*Wait states*
0 (10 MHz)	0	2
0 (10 MHz)	1	1
1 (6 or 8 MHz)	x	1

(x: don't care)

WS2	I	39	Wait states control of 16-bit memory devices on the option card which activates -MEMCS16 signal.
WS3	I	38	

CSPD	*WS3*	*WS2*	*Wait states*
0 (10 MHz)	0	0	4
0 (10 MHz)	0	1	3
0 (10 MHz)	1	0	2
0 (10 MHz)	1	1	1
1 (6 or 8 MHz)	x	x	1

(x : don't care)

A0	I	44	CPU address bus 0.
ALE	I	11	Address latch enables.
-MEMR	I	7	System memory read signal.
-MEMW	I	8	System memory write signal.
-IOR	I	9	System I/O read signal.
-IOW	I	10	System I/O write signal.
-INTA	I	12	Interrupt acknowledge.
-CSRA	I	48	Chip select signal of internal DRAM (0-09FFFF).
-CSRO	I	47	Chip select signal of internal ROM (0E0000-0FFFFF, FE0000-FFFFFF).
-M16	I	17	Chip select signal of 16-bit memory devices on the option slot. (-MEMCS16 signal of option slot is connected to this pin.)
-IO16	I	18	Chip select signal of 16-bit I/O devices on the option slot. (-IOCS16 signal of option slot is connected to this pin.)
IRDY	I	61	I/O channel ready signal. (IOCHRDY signal of option slot is connected to this pin.)
-NPCS	I	45	Chip select signal of numerical processor (80287).
CSPD	I	52	CPU speed select.

CSPD	*CPU speed*
0	10 MHz
1	6 or 8 MHz

TABLE 2-45. (Continued)

Q1	O	2	Q1 signal is active from phase 2 of first Tc cycle to phase 1 of last Tc cycle.
-ARFY	O	25	Asynchronous ready.
-AREN	O	16	Asynchronous ready enable.
COFF	O	60	Control off. This signal becomes active during 16 < -> 8 conversion. While COFF is active, control signals (-EMR, -MEMW, -IOR, -IOW) are disabled.
LSA0	O	23	Latched and converted address 0.
-AEN1	I	43	DMA channel 1 (8-bit DMA) address enable.
-AEN2	I	42	DMA channel 2 (16-bit DMA) adress enable.
-DAEN	O	32	DMA enable. (channel 1 and channel 2)
XA0	Bus	49	Internal address bus 0.
-XBHE	Bus	35	Bus high enable.

-AEN1	*-AEN2*	*XA0*	*-XBHE*
1	1	input	input
0	1	input	- XA0 (output)
1	0	0 (output)	0 (output)

DEN	I	5	Data bus enable.
DTR	I	4	Data transmit ot receive. When HIGH, data is trans-mitted from CPU to memory or I/O.
-GDL	O	57	Enable control of CPU data bus low byte buffer (in GAATDB).
-GDH	O	56	Enable control of CPU data bus high byte buffer (in GAATDB).
-G245	O	54	Enable control of 16 < -> 8 conversion buffer (in GAATDB).
D245	O	55	Direction control of 16 < -> 8 conversion buffer (in GAATDB).
MIO	I	14	Memory or I/O select. CPU M/-IO signal is connected to this pin. When HIGH, memory cycle is being executed.
CDLY	O	59	Command delay. While active, the start of commands (-MEMR, -MEMW, -IOR, -IOW) are delayed.

CSPD	*AREA*	*Command delay*
0 (10 MHz)	16-bit memory	0
0 (10 MHz)	other	1
1 (6,8 MHz)	16-bit memory	0
1 (6,8 MHz)	other	0.5

OUT1	I	21	OUT1 signal of 8254 (Timer LSI)
HRQ1	I	22	Hold request input from 8237 (DMAC LSI).
-XMW	I	46	Internal memory write signal.
HRQ	O	30	Hold request output to CPU.
HLDA	I	3	Hold acknowledge input from CPU.
HAK1	O	31	Hold acknowledge output to 8237 (DMAC LSI).
-RFNO	O	28	Refresh signal. This signal is generated in GAATRF.
-RFNI	I	63	Refresh signal input.
RFPO	O	24	Refresh signal.

TABLE 2-45. (Continued)

-RF1D	O	37	Refresh signal which is delayed by one DMA clock cycle from RFNI signal.
-RF2D	O	36	Refresh signal which is delayed by two DMA clock cycles from RFNI signal.
-DMMR	I	41	DMA memory read signal.
-XIOR	I	50	Internal I/O read signal.
DRDY	O	29	DMA ready signal.
-XMR	Tri	64	Internal memory read signal.
CA20	I	34	CPU address bus 20. A20 signal of CPU is connected to this pin.
A20G	I	33	Gate signal of A20. P21 signal of 8042 (one chip CPU) is connected to this pin.
A20	Tri	62	System address bus 20.

CA20	*A20G*	*A20*	
0	1	0	
1	1	1	
x	0	0	(x: don't care)

CLK	I	51	Processor clock.
SCLK	I	6	System clock.
DCLK	I	13	DMA clock.

CPU speed	CLK	SCLK	DCLK
6 MHz	12 MHz	6 MHz	3 MHz
8 MHz	16 MHz	8 MHz	4 MHz
10 MHz	20 MHz	10 MHz	5 MHz

-RST	I	20	Reset input.
RSTO	O	19	Reset output.
-TEST	I	53	Test input.

* Legend:
I = Input Pin
O = Output Pin
Tri = Output / High-Impedance Pin
Bus = Input / Output / High-Impedance Pin

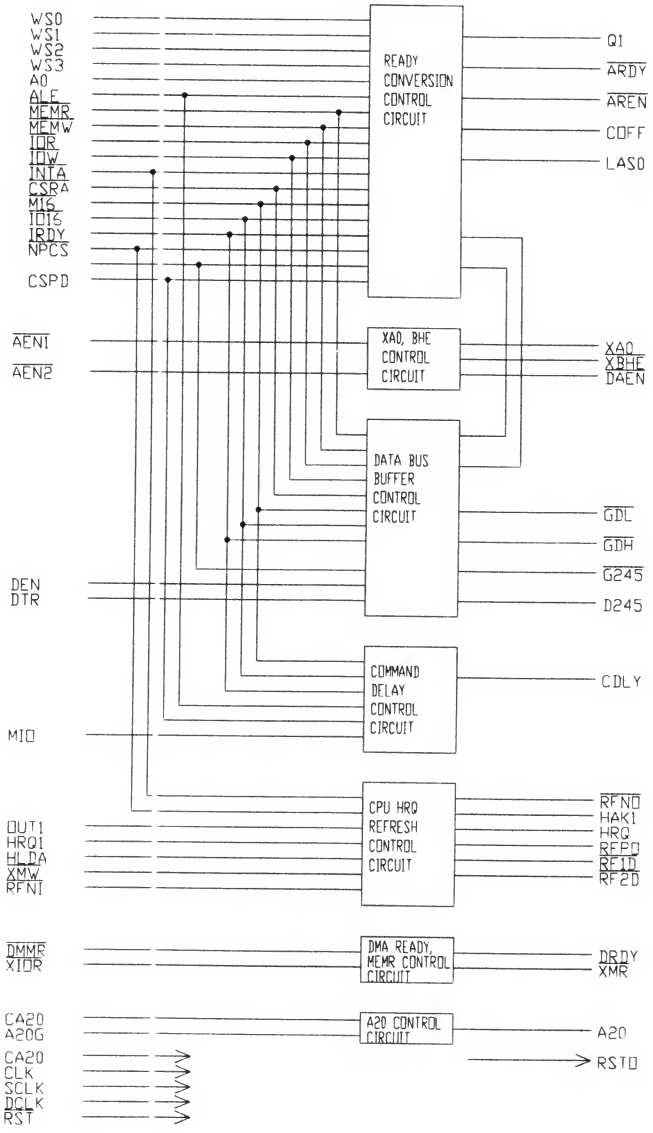


FIGURE 2 – 77. GAATRF INTERNL BLOCK DIAGRAM

2.6.9 GAATSP

GAATSP includes the following functional blocks.

1. Address decoder for serial port (UART, 16450 or 8250)
2. Parallel port. (PTDR: printer data register,
   PTSR: printer status register,
   PTCR: printer control register)
3. Oscillator for UART. (1.8432 MHz output)
4. General purpose 3 – state gate.

GAATSP Pinout Diagram

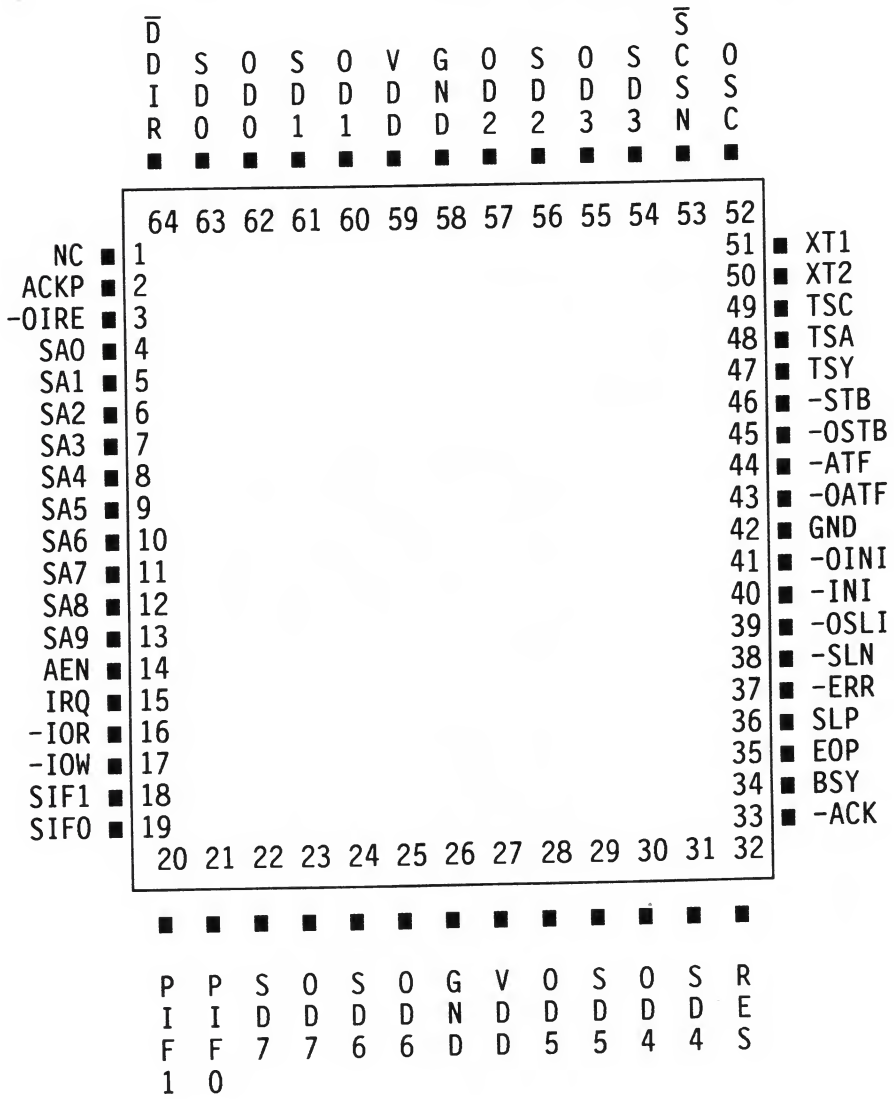


TABLE 7-46. GAATSP PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
SA9-0	I	13-4	Address bus
SD7-0	Bus	22,24,29,31 54,56,61,63	Data bus
-IOW	I	17	I/O write pulse.
-IOR	I	16	I/O read pulse.
AEN	I	14	Address enable. This signal becomes HIGH, when DMA cycle is being executed.
RES	I	32	Reset.
PIF1	I	20	Address select pin for parallel port.
PIF0	I	21	Address select pin for parallel port.

PIF1	*PIF0*	*Parallel port address*
1	1	378, 379, 37A
1	0	278, 279, 27A
0	1	3BC, 3BD, 3BE
0	0	disable

SIF1	I	18	Address select pin for serial port.
SIF0	I	19	Address select pin for serial port.

SIF1	*SIF0*	*Serial port address*
1	1	3F8 - 3FF
1	0	2F8 - 2FF
0	1	disable
0	0	disable

XT1		51	Crystal input. (3.6864 MHz)
XT2		50	Crystal input. (3.6864 MHZ)
OSC	O	52	1.8432 MHz clock output.
TSA	I	48	Data input of 3-state buffer.
TSC	I	49	Control input of 3-state buffer.
TSY	Tri	47	Output of 3-state buffer.
OD7-0	O	23,25,28,30 55,57,60,62	Printer data bit 7-0.
-OSLI	O	39	Printer select.
-OINI	O	41	Printer initialize.
-OATF	O	43	Auto feed.
-OSTB	O	45	Printer data strobe pulse.
-SLN	I	38	Printer select.
-INI	I	40	Printer initialize.
-ATF	I	44	Auto feed.
-STB	I	46	Printer data strobe pulse.
BSY	I	34	Printer busy.
-ACK	I	33	Acknowledge.
EOP	I	35	End of paper.
SLP	I	36	Printer select.
-ERR	I	37	Printer error.
IRQ	Tri	15	Interrupt request. IRQ becomes active, when -ACK becomes LOW and interrupt request is enabled.

TABLE 2 – 46. (Continued)

– OIRE	O	3	Interrupt request enable.
ACKP	O	2	Acknowledge.
– SCS	O	53	Chip select signal of serial port.
– DDIR	O	64	Direction control of data buffer. This signal is active while serial port or parallel port are being read.

* Legend: I = Input Pin
O = Output Pin
Tri = Output / High – Impedance Pin
Bus = Input / Output / High – Impedance Pin

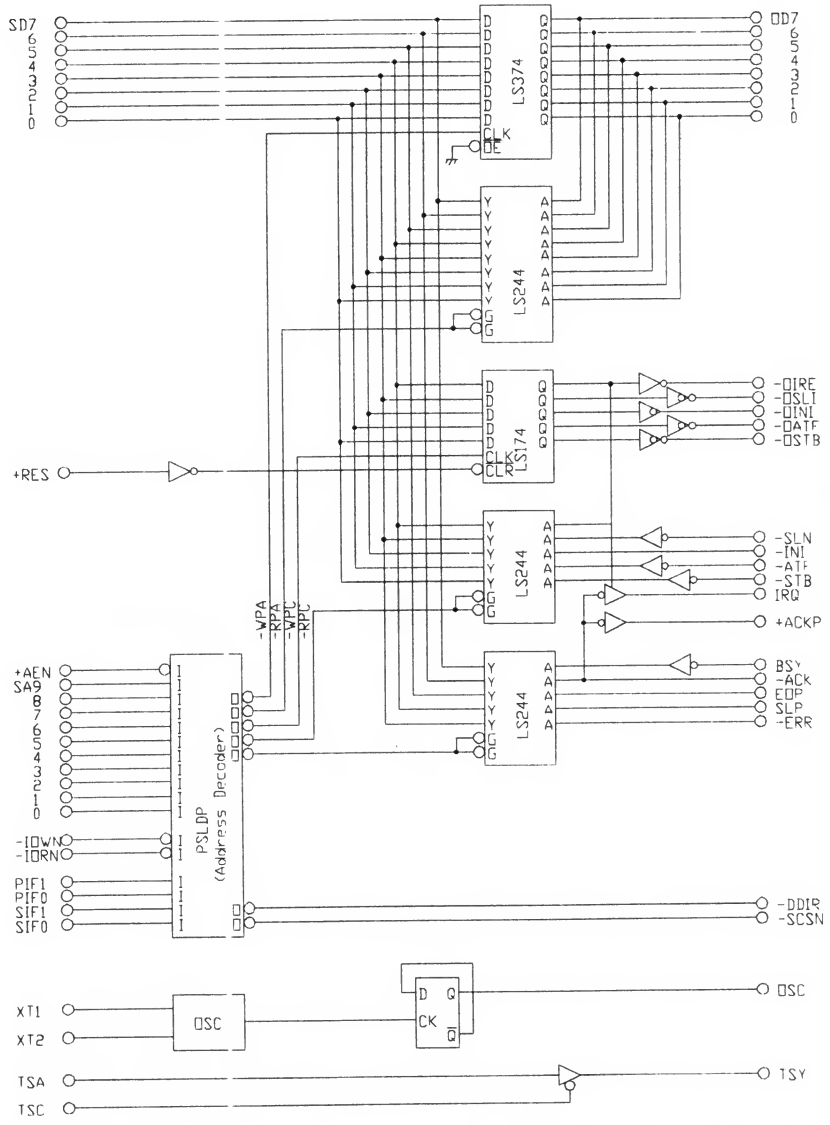


FIGURE 2 – 78. GAATSP INTERNAL BLOCK DIAGRAM – I

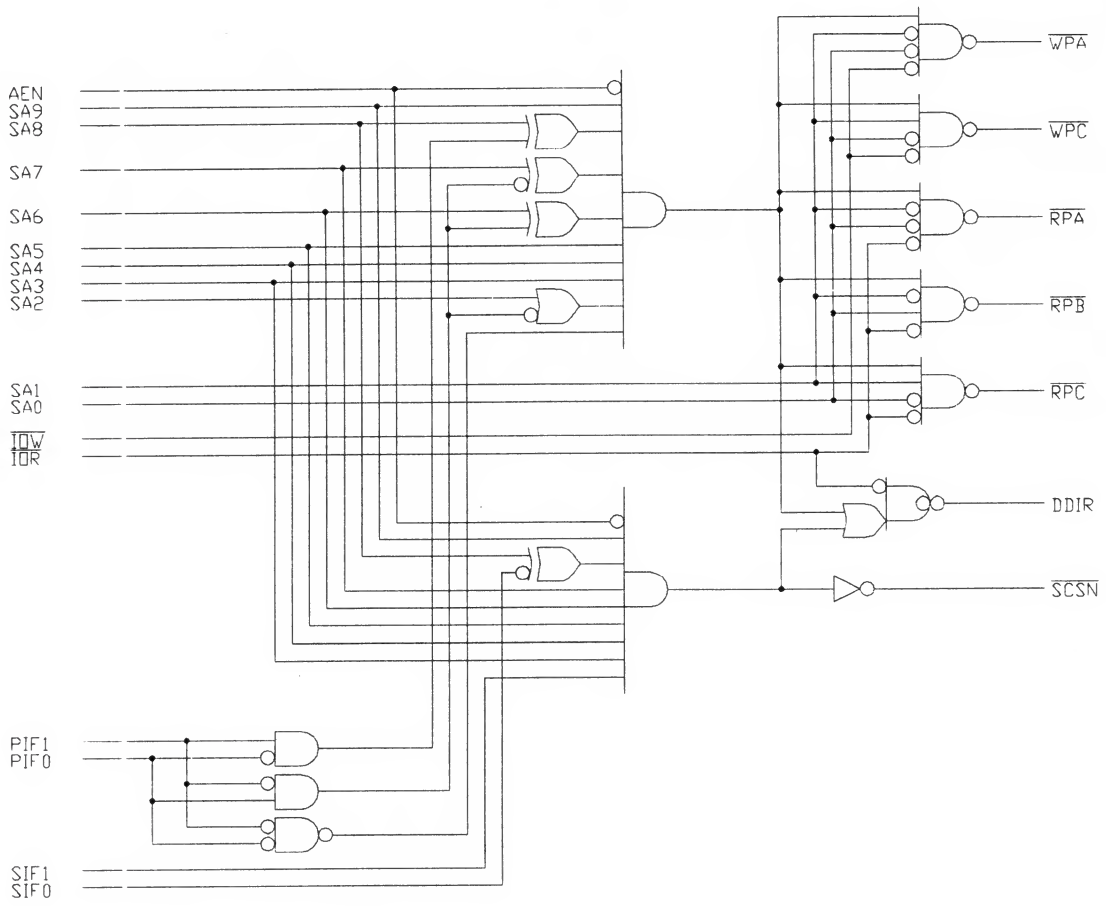


FIGURE 2 – 79. GAATSP INTERNAL BLOCK DIAGRAM – II

2.6.10 GAATCX

GAATCX includes following functional blocks.

1. Clock generator
   CPU clock (24MHz, 20MHz, 16MHz, 12MHz)
   14.31818 MHz
2. Clock selector
   CPU clock is selected By a slide switch (without reboot).
   CLKO : 12MHz <–> 16MHz <–> 20MHz or 24MHz

GAATCX Pinout Diagram

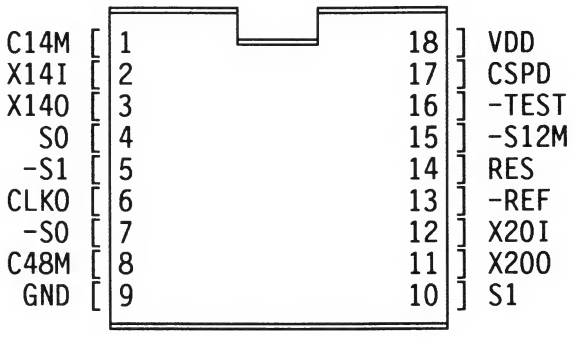


TABLE 2–47. GAATCX PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
C48M	I	8	48MKHz clock input
X20I	I	12	Oscillator input (20MHz)
X20O	O	11	Oscillator output
X14I	I	2	Oscillator input (14.31818MHz)
X14O	O	3	Oscillator output
C14M	O	1	14.31818MHz clock output
CLKO	O	6	CPU clock output
SO	I	4	Clock select 0
–SO	I	7	Clock select 0
S1	I	10	Clock select 1
–S1	I	5	Clock select 1
–S12M	I	15	Clock select (20MHz <–> 24MHz)

SO	*–SO*	*S1*	*–S1*	*–S12M*	*CLKO*
1	0	0	1	*	12MHz
1	0	1	0	*	16MHz
0	1	1	0	1	20MHz
0	1	1	0	0	24MHz

TABLE 2-47. (Continued)

-RES	I	14	Reset signal input
-REF	I	13	Refresh signal input
CSPD	O	17	Clock speed signal

CSPD	*CLKO*
1	12MHz or 16MHz
0	10MHz or 24MHz

* Legend: I = Input Pin
O = Output Pin

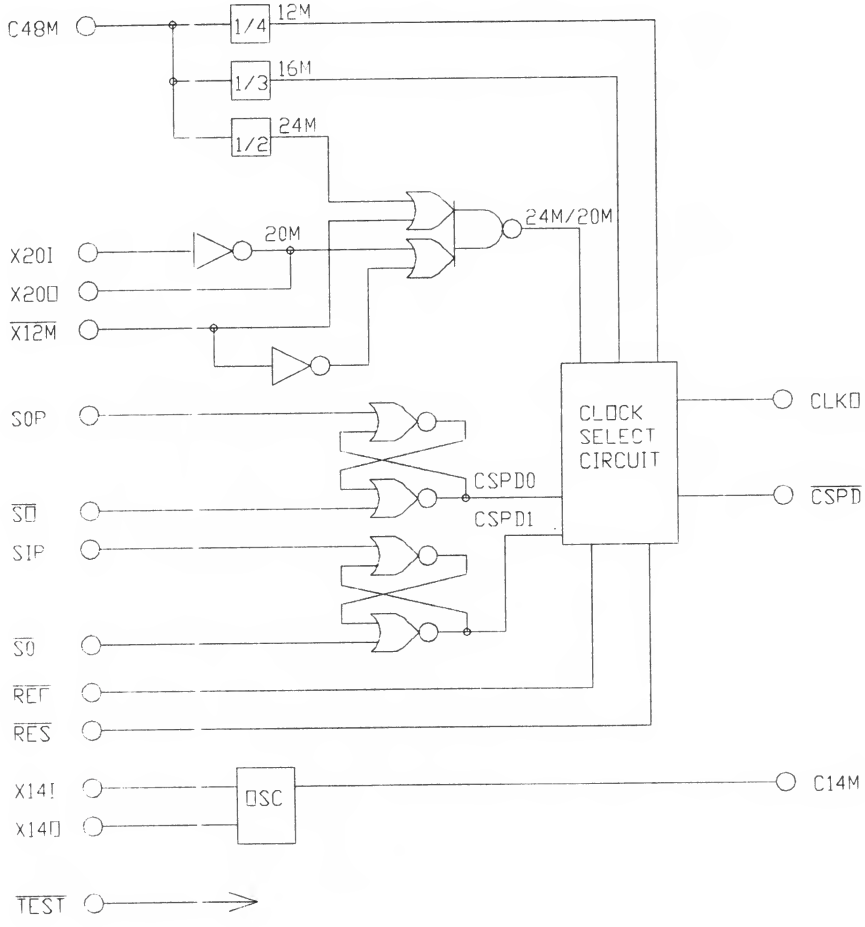


FIGURE 2-80. GAATCX INTERNAL BLOCK DIAGRAM

2.6.11 WD37C65 FLOPPY DISK SUBSYSTEM CONTROLLER

The WD37C65 floppy disk subsystem controller is an LSI device that provides all the needed functionality between the host processor peripheral bus and the cable connector to the floppy disk drive. This 'superchip' integrates: Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive Interface Drivers and Receivers.

WD37C65 Pinout Diagram

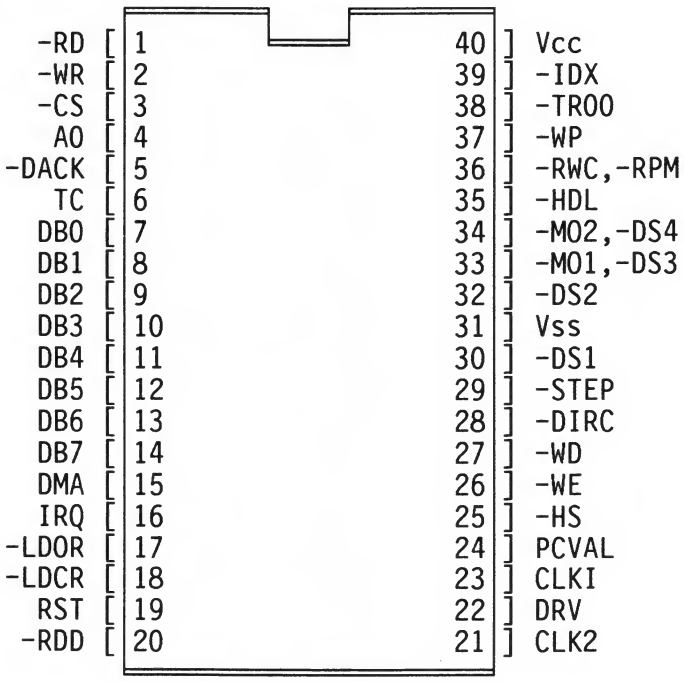


TABLE 2-48. WD37C65 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
-RD	I	1	Control signal for transfer of data or status onto the data bus by the WD37C65.
-WR	I	2	Control signal for latching data from the bus into the WD37C65 buffer register.
-CS	I	3	Chip Select signal.
A0	I	4	Address line 1.
-DACK	I	5	DMA Acknowledge signal.
TC	I	6	Terminal Count. This signal indicates to WD37C65 that data transfer is completed.
DB0-DB7	I/O	7 - 14	8-bit, bi-directional, tri-state, data bus.
DMA	O	15	DMA request for byte transfers of data.
IRQ	O	16	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode).
-LDOR	I	17	Load Operations Register. Address decode which enables the loading of the Operations Register.
-LDCR	I	18	Load Control Register. Address decode which enables loading of the Control Register.
RST	I	19	Reset signal.
-RDD	I	20	Read Disk Data.
CLK2	I	21	9.6MHz clock input.
DRV	I	22	Drive type signal.
CLK1	I	23	16 MHz clock input.
PCVAL	I	24	Precompensation Value select signal. Determines amount of write precompensation on inner tracks of diskette. HIGH = 125ns; LOW = 187ns.
-HS	O	25	Head select signal. "1"= side 0, "0"= side 1
-WE	O	26	Write Enable Signal.
-WD	O	27	Write data.
-DIRC	O	28	Direction signal.
-STEP	O	29	Step pulse.
-DS1	O	30	Drive select 1.
Vss	-	31	Ground.
-DS2	O	32	Drive select 2.
-MO1, -DS3	O	33	Motor on 1, Drive select 3.
-MO2, -DS4	O	34	Motor on 2, Drive select 4.
-HDL	O	35	Head loaded signal.
-RWC, -RPM	O	36	Reduced write current, Revolutions per minute.
-WP	I	37	Write protected signal.
-TR00	I	38	Track 00 signal.
-IDX	I	39	Index signal.
Vcc	-	40	+5V DC.

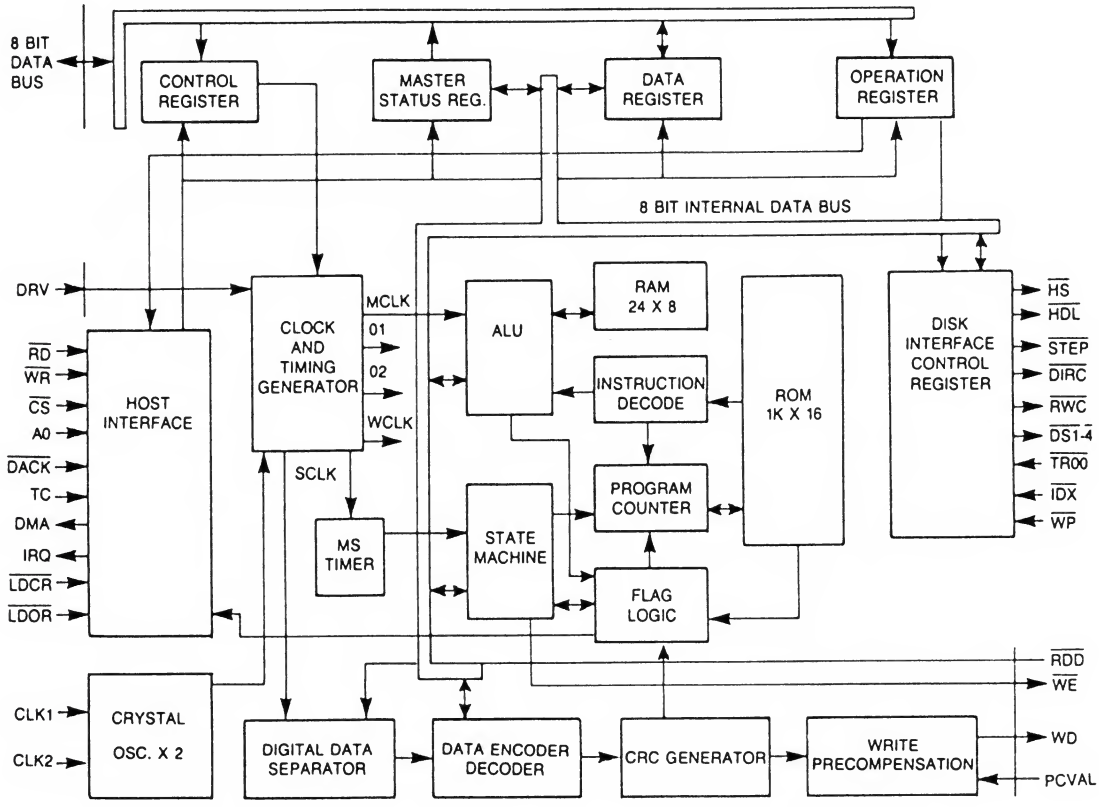


FIGURE 2-81. WD37C65 INTERNAL BLOCK DIAGRAM

2.6.12 NS16450 ASYNCHRONOUS COMMUNICATIONS ELEMENT

The NS16450 is an improved specification version of the INS8250A Asynchronous Communications Element.

The serial-interface characteristics are fully programmable as follows:

- 5-, 6-, 7- or 8-bit characters
- Even, odd, or no-parity bit generation and detection
- 1-, 1.5-, or 2-stop bit generation
- Baud generation (DC to 56k buad)

NS16450 Pinout Diagram

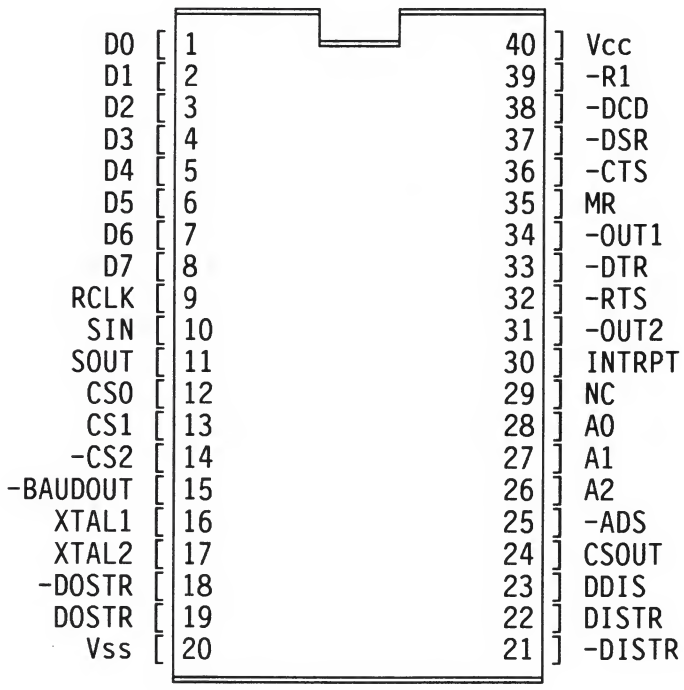


TABLE 2-49. NS16450 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
CS0,CS1.	I	12,13	Chip select signals.
-CS2		14	
DISTR,	I	22	Data input strobe.
-DISTR		21	
DOSTR,	I	19	Data output strobe.
-DOSTR		18	
-ADS	I	25	Address strobe signal.
A0-A2	I	26-28	Register select signal.
MR	I	35	Master reset signal.
RCLK	I	9	Receiver clock.
SIN	I	10	Serial data input from the communications link.
-CTS	I	36	Clear to send.
-DSR	I	37	Data set ready.
-DCD	I	38	Data carrier detect.
-RI	I	39	Ring indicator.
Vss	-	20	Ground.
-DTR	O	33	Data terminal ready.
-RTS	O	32	Request to send.
-OUT1	O	34	User-designated output that can be set to an active LOW by programming bit 2 (OUT 1) of the modem control register to a HIGH level.
-OUT2	O	31	User-designated output that can be set to an active LOW by programming bit 3 (OUT 2) of the modem control register to a HIGH level.
CSOUT	O	24	Chip select out.
DDIS	O	23	Driver disable.
BAUDOUT	O	15	Baud out signal.
INTRPT	O	30	Interrupt request signal.
SOUT	O	11	Serial output signal.
D7-D0	I/O	1-8	Eight bit tri-state input/out data bus.
XTAL1,XTAL2	I/O	16,17	External clock input/output.
Vcc	-	40	+5V DC.

* Legend: I = Input Pin
O = Output Pin

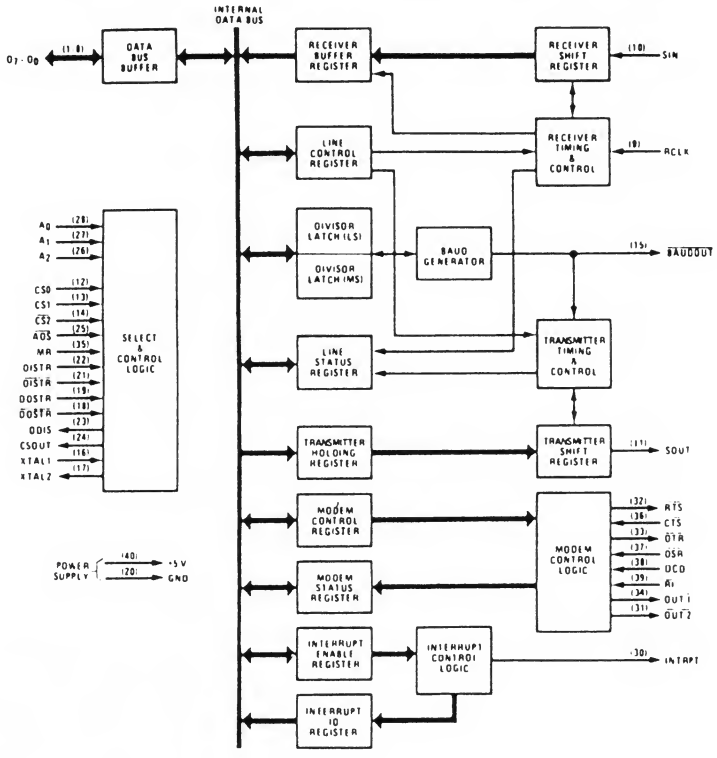


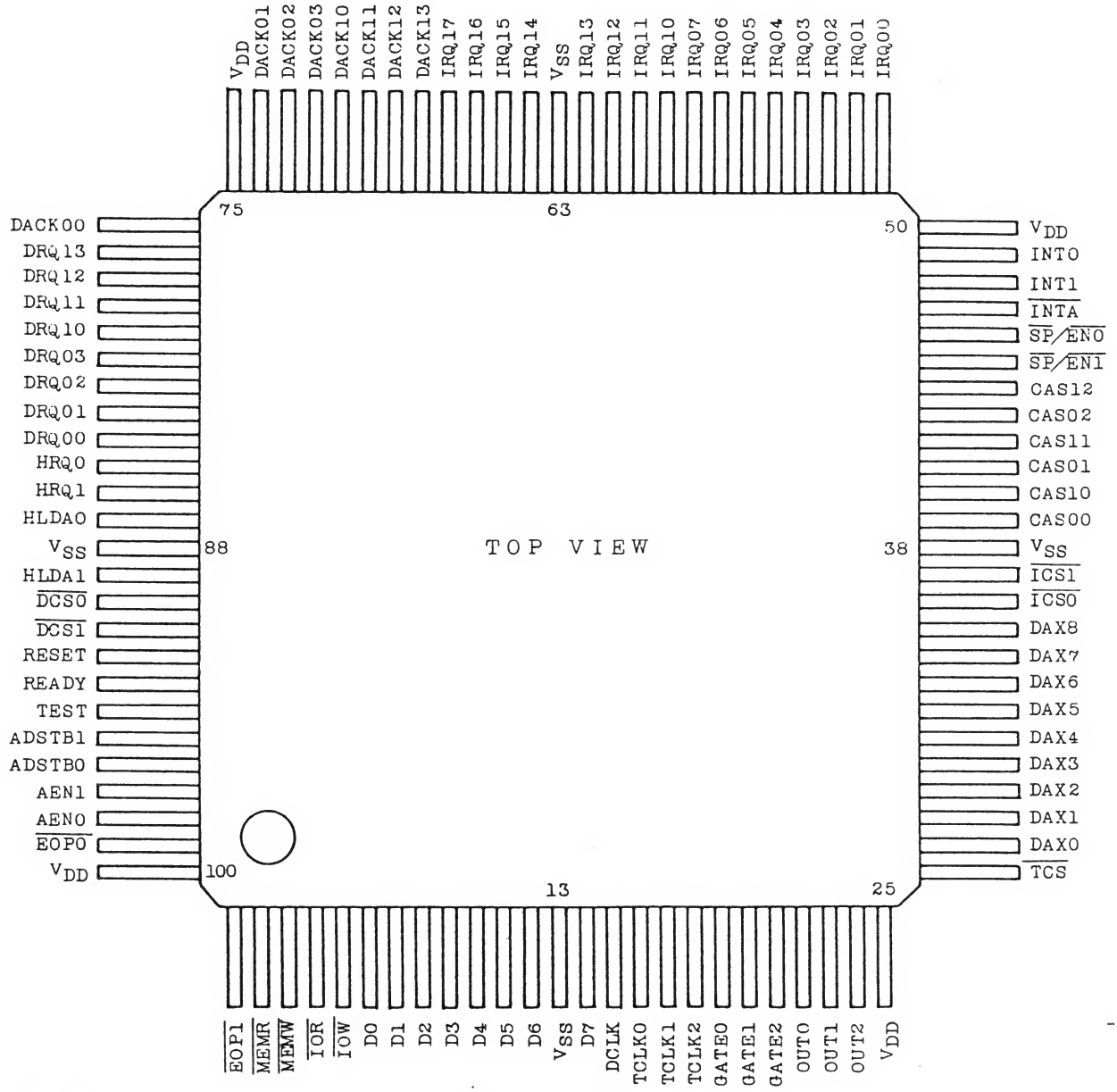
FIGURE 2 – 82. NS16450 INTERNAL BLOCK DIAGRAM

2.6.13 T4758 SUPER INTEGRATED CHIP

A super integtated chip T4758 combines and includes the following five chips.

Counter/Timer ..... One 8254 (3 channels)
DMA controller ..... Two 8237A (8 channels)
Interrupt controllrer .... Two 8259A (16 levels)

T4758 ***Pinout Diagram***



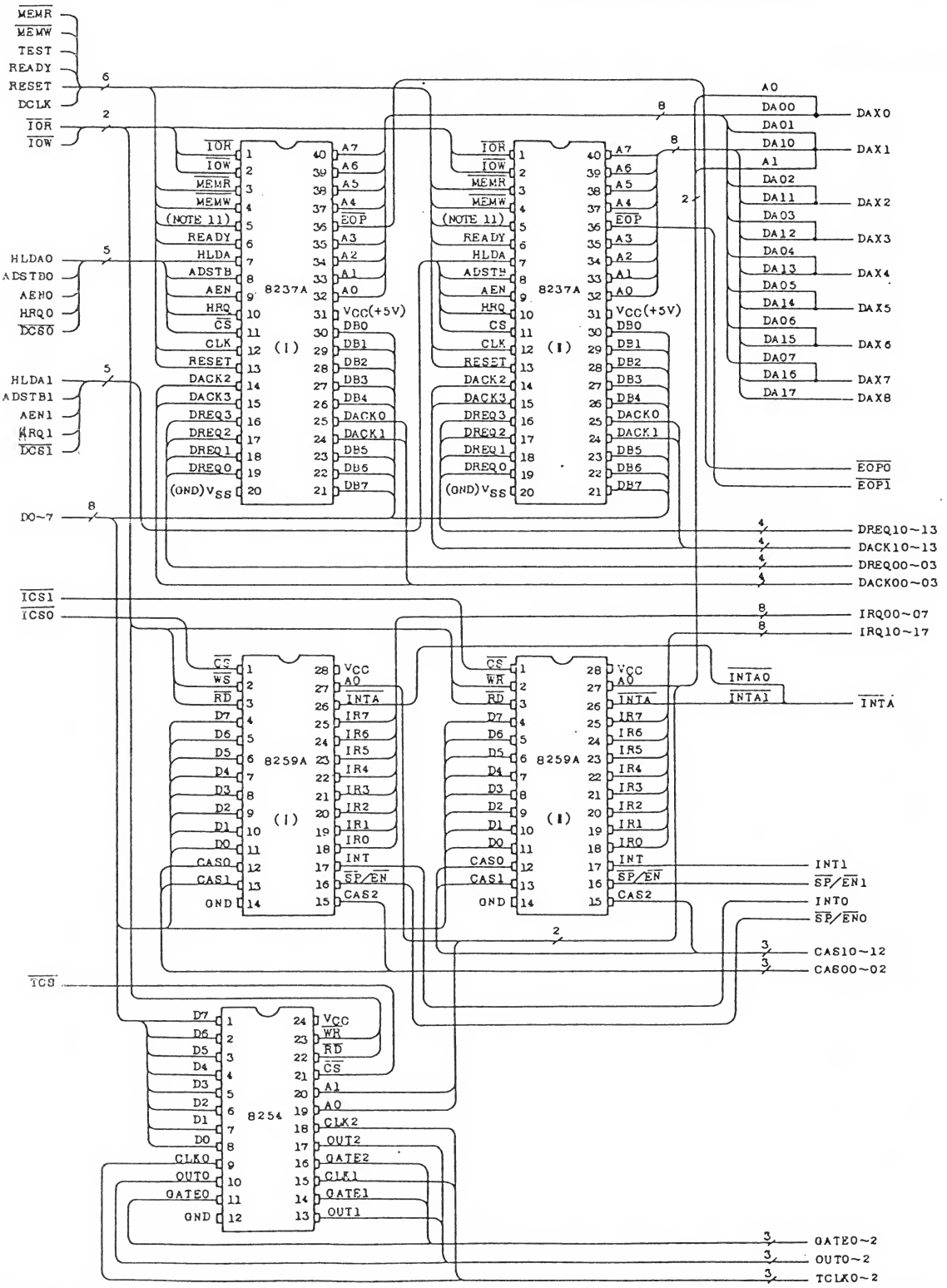


FIGURE 2 – 83. T4758 INTERNAL BLOCK DIAGRAM

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OPTIONS

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4.1 SERVICE TOOLS

Recommended service tools are listed in Table 4 – 1 with corresponding EPSON part numbers; these are also commercially available.

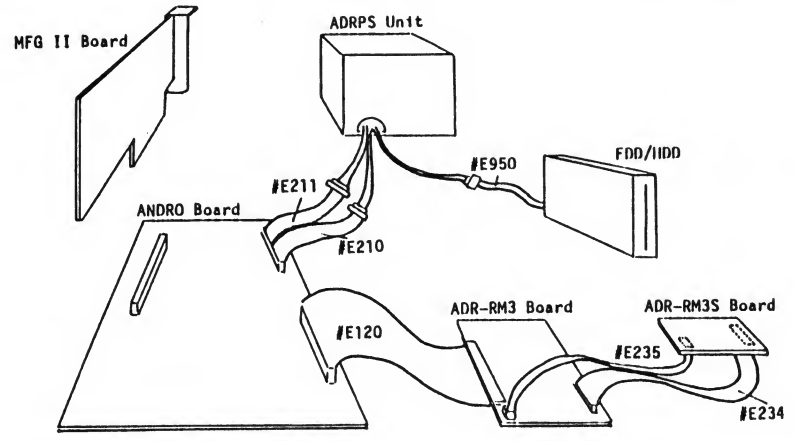


FIGURE 4 – 1. CONNECTION OF SERVICE TOOLS

TABLE 4 – 1. SERVICE TOOL LISTING

Tool Name	*Part No.*	*Description*
MFG BOARD	B778601701	Bus status check board.
MFG2 BOARD	B777605801	Assistant board for troubleshooting
CABLE #E210	B778602001	Expansion for power supply between ADRPS unit (CN2) and ANDRO board (CN13)
CABLE #E211	B778602101	Expansion for power supply between ADRPS unit (CN1) and ANDRO board (CN12)
CABLE #E950	Y130327000	Expansion for power supply between ADRPS unit (CN3/4/5) and FDD/HDD
CABLE #E120	B777601201	Expansion for connection between ANDRO board (CN7) and ADR – RM3 board (CN1)
CABLE #E234	B777605601	Expansion for connection between ADR – RM3 board (CN2) and ADR – RM3S board (CN1)
CABLE #E235	B777605701	Expansion for connection between ADR – RM3 board (CN3) and ADR – RM3S board (CN2)

4.2 Power – On Diagnostics (POD)

4.2.1 GENERAL DESCRIPTION

The ROM BIOS has routines that carry out tests of the installed hardware. The hardware present is also checked against the configuration byte in CMOS RAM. These routines are referred to as Power On Diagnostics (POD).

The 80286 CPU is reset when the power is turned on or the reset button pushed, and when CTRL + ALT + DEL are pressed at the same time. Upon reset, the system begins execution starting at the reset vector address 0FFFF:0000. The POD begin at this point.

The system initialization which begins at the power – on reset vector is responsible for performing the self tests and initializing the I/O devices, testing the system RAM, and then initializing the contents of BIOS variables. Note that the RAM is tested only during power – on initialization, and not when reset is caused by pressing CTRL + ALT + DEL.

The programmable I/O devices that are tested during initialization include the interrupt con – trollers, the DMA controllers, the keyboard and display controllers, the timer/counter, the floppy – disk and hard – disk controllers, and the serial and parallel adapters.

The memory initialization that is performed at power – on time consists of tests on the BIOS ROM and the system RAM areas. These tests detect any mulfunctioning memory devices.

The ROM BIOS is tested using a checksum, and the test must be successful for the power – on initialization sequence to continue. If a ROM check – sum error occurs, power – on initalization stops and the CPU halts.

The first part of the system RAM test checks that the first 64K bytes are fully operational. The initalization procedures use this area for stack and variable storage.

The final initalization step performs an INT 19h which loads and transfers control to the operating system. This interrupt loads the boot sector on the floppy – disk or hard – disk. If the boot sector is not valid, the routine prompts the user to retry with another operating system disk.

4.2.2 SUMMARY OF POD TEST PROCEDURES

Before each test, the POD writes a code that identifies the test (called the "step ID") into a special 8 – bit I/O port at address 80h – the "POD step port".

If the POD detects a fatal error, it halts the system; otherwise it displays a warning message and takes one of two actions. If the Diagnostics Error Ignore function has been set for the test that failed, execution continues immediately. If not, the *"F1" to resume* message is displayed, and the user must press F1 to continue with the tests. The error ignore function is described in detail below. In either case, a special POD function can access the step ID at port address 80h and display it on the CRT (see below).

THE POD STEP ID

When the system is powered up the POD tests are performed sequentially from 01h to 51h, and the step ID is set to these values in turn. The step ID may also be set to 81h when switching to

protected mode, or to a value in the range 90h – B6h should an exception occur in protected mode. The remaining values are reserved for future tests.

FATAL ERRORS

When the CPU halts due to a fatal error in the POD, the POD step ID can be displayed on the CRT as a hexadecimal value. Refer to the detailed list of POD step IDs below for more information on each error.

To display the step ID, reverse the setting of the monitor – type select switch on the front panel. The POD step ID is then displayed on the CRT. There are two cases when this procedure does not work: when the error is in the 8042 keyboard controller or video card, or when an enhanced graphics adapter is installed.

4.2.3 DIAGNOSTICS ERROR IGNORE FUNCTION

This function allows the user to selectively ignore certain non – fatal errors. The selected error conditions to be skipped are indicated in CMOS RAM, bytes 34h – 3Fh.

The data to enable this function are:

34h – 3Dh	filled with the string skip marker	SEIKOEPSON
3E,3Fh	specified error condition bits set	

If the bit corresponding to an error is 0, the "F1" request is skipped. Otherwise, if an error occurs and the corresponding bit is 1 then the "F1" key is requested as normal.

4.2.4 ADDING NEW POD TESTS

If the POD needs additional test procedures, then an unused step ID can be used. MajorPOD steps will use IDs in the range 52h – 6Fh; minor steps in protected mode will use one of the unused step IDs from 80h – FFh.

4.2.5 QUICK BOOT

When the full POD is carried out many devices are tested. The memory check and the HDD retries caused by an HDD error (for example, wrong HDD type, or unformatted drive) take a long time.

To skip the memory check and HDD retries, press the left side ALT key while turning on the power, or while pressing the reset button. Keep the key pressed for about 1 second before releasing it. The remaining tests that are performed are part of a POD function called 'Quick Boot'. When a keyboard reset is performed, Quick Boot is always used.

When Quick Boot is performed:

- the memory-size determination section (the visible memory count up) is skipped;
- multiple retries to initialize each HDD are disabled (only one retry is allowed per drive, instead of 1 minute per drive);
- the stuck-key test does not fail due to the ALT key (38h) being held down.

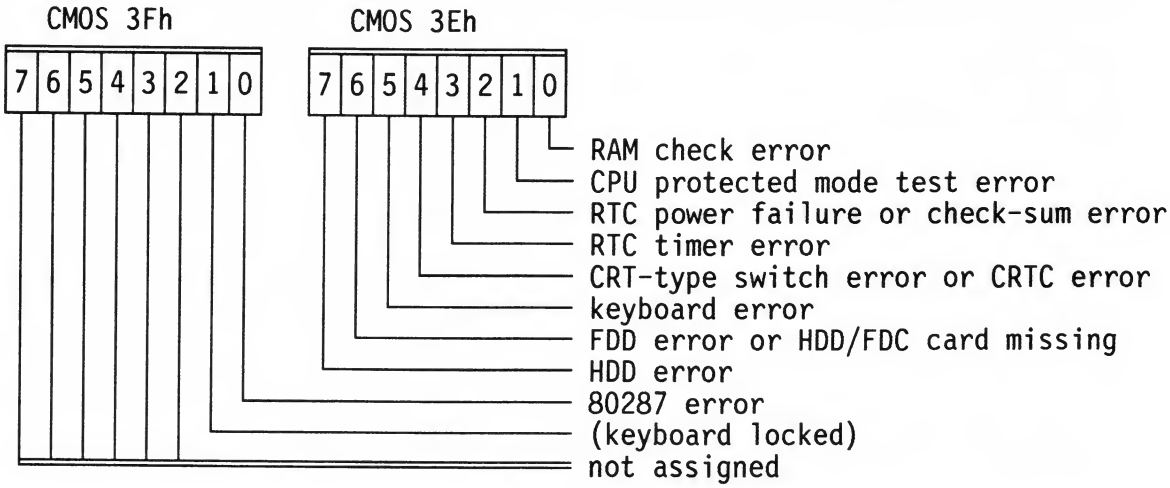


FIGURE 4-2. ERROR IGNORE BITS

4.2.6 COMPATIBILITY BETWEEN DIFFERENT PROCESSORS

When the POD is complete, the IOPL and NT flags are cleared to provide compatibility between the 80286 and 80386. The state of certain flags can also be used by an application to determine the processor type.

286/386 COMPATIBILITY:

The 80286 cannot change the IOPL and NT flags in real mode, unlike the 80386. This means that when IOPL or NT changes as a result of some operation or application that changes into protected mode, problems can occur if the 80286 or user expects IOPL=0 and NT=0.

Note that INT 15h, AH=89h (change to virtual mode) changes from real to protected mode with IOPL=0 and NT=0. On the other hand, INT 15h, AH=87h (move memory block) does not change the current IOPL and NT status.

DETERMINING PROCESSOR TYPE:

It is possible to determine whether the installed CPU has a protected mode or not by direct reflection of the flags register in real mode. If required, the exact processor type can be

determined. To perform the determination, use the simple procedure shown below. The contents of BX on exit can be used to interpret the processor type.

PROCESSOR TYPE TEST ROUTINE:

```
mov  ax,CONSTANT        ; use 0000h or 0FFFFh for test
push ax                 ; push CONSTANT onto stack
popf                    ; pop CONSTANT into flags register
pushf                   ; push flags back onto stack
pop  bx                 ; transfer flags register value to BX
```

TABLE 4-2. PROCESSOR TYPE RETURN VALUES IN BX

CPU type	*CONSTANT*	*Copy of flags in BX*	*Notes*
80386	0FFFFh	0111 1110 1101 0111	Top 4 bits vary
	00000h	0000 0000 0000 0010	according to CONSTANT
80286	0FFFFh	0000 1110 1101 0111	Top 4 bits always 0
	00000h	0000 0000 0000 0010	
8086/88	0FFFFh	1111 1110 1101 0111	Top 4 bits always 1
	00000h	1111 0000 0000 0010	

4.2.7 POD STEP ID NUMBERS

Mode Change	STEP ID Normal	STEP ID Fail only	Contents
	??		test all flags reset IOPL=0, NT=0
	01h		test MSW.PE= =0 in real mode
	02h		(reserved) IF and DF test
	03h		VIDEO initialization and disable parity check
	04h		BIOS ROM checksum disable RTC interrupt
	05h		DMA page register test DMA page registers are all set to 00h
	06h		verify CMOS restart byte CMOS(0fh) and reset restart byte= =0

07h	disable DMA controller #1 & #2 Counter 1: high nibble does not become 0000xxxx
08h	Counter 1: high nibble does not become 1111xxxx
09h	check RAM refreshing RAM refresh detect bit == 1
0Ah	RAM refresh detect bit == 0
0Bh	test DMA controller #1
0Ch	test DMA controller #2
0Dh	initialize DMA controller #1, #2
0Eh	initialize #1 CH0-CH3, #2 CH5-CH7
0Fh	test base 64K bytes RAM
10h	if fail on 0Fh then check E-VIDEO ROM
11h	initialize E-VIDEO controller if fail on 0fh then display error address
12h	(reserved) check RAM refresh speed
13h	check CMOS(0Ah) value
14h	reset 80287 initialize 8259 #1 & #2
15h	set up interrupt vector 0,1,3,4,6,10h-5Fh,68h-6Fh to temporary routines set up interrupt vector 10-1Fh
16h	test 8042 (keyboard controller)
17h	issue 8042 self test command and verify result
18h	read input port data and save
19h	first setup to keyboard controller
1Ah	check CMOS power status and checksum
1Bh	if fail on 1Ah then write status into CMOS(0Eh)
1Ch	toggle keyboard port to reset keyboard system check keyboard stuck

	1Dh	determine equipment and VIDEO mode
	1Eh	set up VIDEO mode
	1Fh	test CRT controller
	20h	verify E-VIDEO ROM
	21h	if fail on 1Eh, 1Fh then VIDEO setting error
	22h	verify word access to I/O PORT
	23h	test interrupt controller #1 verify interrupt mask register #1
	24h	test interrupt controller #2 verify interrupt mask register #2
	25h	test interrupt occur when all masked #1 & #2
	26h	test counter 0
	27h	test counter 0 interrupt is not occur
	28h	test counter 0 interrupt is occur
	29h	set up counter 0
	2Ah	test counter 2
	2Bh	test NMI interrupt (When NMI masked)
	2Ch	test keyboard status port Check keyboard buffer is empty
	2Dh	enter protect mode
R->P	2Eh	verify PE bit == 1 in protect mode
	2Fh	test memory size on system board (0-512K)
	30h	test I/O memory size (512-640K, 1024K-???K)
	31h	prepare to test address line 19-23
	32h	verify address line 19-23
P->R	33h	if fail on 32h then RESTART 8 & CPU halt
	34h	finish memory size check

	35h	enter protected mode
R – > P	36h	verify PE = = 1 in protected mode
	37h	determine RAM size
	38h	test RAM
	39h	prepare to verify address line 16 – 23
P – > R	3Ah	verify address line 16 – 23
R – > P	3Bh	verify PE = = 1 in protected mode return immediately from protected to real
P – > R		(untest in protected mode contents)
	3Ch	disable all interrupt mask interrupt mask register
	3Dh	test keyboard controller input buffer will be empty or not
	3Eh	if fail on 3Dh then keyboard clock error detect
	3Fh	test keyboard interface line, check keyboard clock will be low/high perform basic assurance test check output buffer will be empty
	40h	enable and setup keyboard parameters
	41h	set up all interrupt vector
	42h	display CRT setting error message enable timer 0 interrupt (IR0) verify RTC clock
	43h	test FDD & HDD (Entry point of Boot Strap Loader)
	44h	invoke FDD initialize routine
	45h	invoke HDD initialize routine
	46h	enable DMA #4 channel
	47h	set parallel/serial timeout value and number
	48h	I/O ROM check (0C8000 – 0DFFFFh) and invoke their initialize routine

49h	setup system timer
4Ah	initialize keyboard system
4Bh	verify 80287
4Ch	check whether "F1" request needed or not
4Dh	if at 4Ch "F1" was requested, then check keyboard LOCK status
4Eh	clear DMA page register
4Fh	test expansion ROM (0E000:00000 - 0E000:0FFFF)
50h	invoke expansion ROM initializer
51h	IPL
(43h	Entry point of Boot Strap Loader)

Note: The Mode Change column shows where the POD switches the CPU from real mode to protected mode or vice versa.

4.2.8 POD ERROR MESSAGES

The POD tests check the status of the system when it boots up, and respond according to the kind of error.

If the POD finds a fatal error during the check of I/O devices, it writes the step ID to I/O port 80h, and the user can display it as described above. It then halts the system. The POD step ID indicates where the error was found so that appropriate action can be taken.If the POD finds a minor error, it displays an error message and waits until the F1 key is pressed. The POD step ID is also written to I/O port 80h for reference. The system boots up after the F1 key is pressed, and all devices that tested successfully can be accessed as normal.

The rest of this section describes the POD error messages in detail and suggests the action which may be taken to remedy the problem indicated.

MESSAGE	PORT(80)
(none)	01h

NEXT: HALT
CAUSE: CPU
RESPONSE: Restart or replace CPU
EXPLANATION: The Protection Enable (PE) bit in the CPU machine status word MSW was 1 instead of 0.

MESSAGE	PORT(80)
(none)	04h

NEXT: HALT
CAUSE: BIOS ROM
RESPONSE: Replace ROM BIOS
EXPLANATION: An error occurred in the ROM BIOS checksum.

MESSAGE	PORT(80)
(none)	05h

NEXT: HALT
CAUSE: GAATIO
RESPONSE: Replace GAATIO
EXPLANATION: An error occurred during a DMA page register check operation.

MESSAGE	PORT(80)
(none)	06h

NEXT: HALT
CAUSE: 146818 (RTC)
RESPONSE: Replace RTC
EXPLANATION: An error occurred during the RTC CMOS RAM area 0Fh (shutdown status byte) check operation. Checking is performed by setting and verifying each bit sequentially.

MESSAGE	PORT(80)
(none)	07h or 08h

NEXT: HALT
CAUSE: 8254
RESPONSE: Replace 8254
EXPLANATION: An error occurred in timer/counter 1.

– For 07h:

A 1 is written in each bit of the counter register and counting is started. An error occurs if all four upper bits of the counter become zeros.

– For 08h:

A 0 is written in each bit of the counter register and counting is started. An error occurs if all four upper bits of the counter become 1.

MESSAGE	PORT(80)
(none)	09h or 0Ah

NEXT: HALT
CAUSE:
RESPONSE:
EXPLANATION:
I/O port 61h Refresh detect bit: Half of the refresh signal frequency is indicated by this bit.
– For 09h:
I/O port 61h bit 4 did not become 0.
– For 0Ah:
I/O port 61h bit 4 did not become 1.

MESSAGE	PORT(80)
(none)	0Bh or 0Ch

NEXT: HALT
CAUSE: 8237A5 (DMAC)
RESPONSE: Replace 8237A5
EXPLANATION:
– For 0Bh:
An error occurred while checking DMA controller 1 (cascade – connected first row) register.
– For 0Ch:
An error occurred while checking DMA controller 2 (cascade – connected second row) register.

MESSAGE	PORT(80)
000000 xxxx 201	11h or error bit pattern

NEXT: HALT
CAUSE: RAM
RESPONSE: Replace RAM
EXPLANATION: An error occurred while checking the lowest 64K bytes of RAM.

MESSAGE	PORT(80)
(none)	16h

NEXT: HALT
CAUSE: 8042 (8742)
RESPONSE: Replace 8042 (8742)
EXPLANATION: The Input Buffer Full (IBF) bit in the 8042 (8742) status register was not cleared even after a fixed time elapsed.

If the IBF bit is set, the 8042 (8742) data bus buffer contains data. The IBF bit is normally automatically cleared by the 8042 (8742) internal program.

MESSAGE	PORT(80)
(none)	17h

NEXT: HALT
CAUSE: 8042 (8742)
RESPONSE: Replace 8042 (8742)
EXPLANATION: The normal termination code (55h) was not returned when the keyboard controller self – test program was executed. Note that the keyboard controller self – test differs from the keyboard unit self – test.

MESSAGE	PORT(80)
(none)	18h

NEXT: HALT
CAUSE: 8042 (8742)
RESPONSE: Replace 8042 (8742)
EXPLANATION: The IBF bit in the 8042 (8742) status register was not cleared even though a fixed time elapsed after a command was sent to the 8042 (8742) data bus buffer.

The IBF bit in the 8042 (8742) status register is set when the data bus buffer contains command or data. The IBF bit is normally automatically cleared by the 8042 (8742) internal program.

MESSAGE	PORT(80)
106-System board error	22h

NEXT: HALT
CAUSE:
RESPONSE:
EXPLANATION: An error was detected while checking access to the DMA page board error register (83, 84h).
The following two check operations are performed:

(1) 55AAh is written as data to I/O port 22h. The data is read back and the test fails if it is different from the data written.

(2) 55AAh is written to I/O port 22h a byte at a time, the data is read back and the test fails if it is different from the data written.

MESSAGE	PORT(80)
101-System board error	23h -- 25h

NEXT: HALT
CAUSE: 8259
RESPONSE: Replace 8259
EXPLANATION: An error occurred while checking the Interrupt Mask Register (IMR).
- For 23h:
  An error was detected in the IMR of the master interrupt controller. Checking is done by writing and verifying 00h and FFh in the IMR.
- For 24h:
  An error was detected in the IMR of the slave interrupt controller. Checking is the same as for 23h.
- For 25h:
  An interrupt occurred even though all bits in the IMR were set. Checking is performed by writing the value FFh to the IMRs of the master and slave interrupt controllers and checking for interrupts by software ST1.

MESSAGE	PORT(80)
102-System board error	26h or 27h

NEXT: HALT
CAUSE: 8254-2, 8259A-2
RESPONSE: Replace 8254-2 or 8259A-2
EXPLANATION: An error was detected in timer controller counter 0.
- For 26h:
  The timer is set so that interrupt occurs after 60µs. An error is indicated if an interrupt does not occur during the next 90µs.
- For 27h:
  The timer is set so that an interrupt occurs after 200µs. An error is indicated if an interrupt occurs during the next 150µs.

MESSAGE	PORT(80)
103-System board error	28h

NEXT: HALT
CAUSE: 8254-2, 8259A-2
RESPONSE: Replace 8254-2 or 8259A-2
EXPLANATION: This error is indicated if a counter 0 interrupt caused by the operation explained for 27h does not occur after 200µs.

MESSAGE	PORT(80)
108-System board error	2Ah

NEXT: HALT
CAUSE: 8254-2
RESPONSE: Replace 8254
EXPLANATION: The value 55AAh is written in timer controller counter 2, the counter is read, and the data is compared with the data written. An error is indicated if the data written is not equal to the data read.

MESSAGE	PORT(80)
105-System board error	2Bh

NEXT: HALT
CAUSE: RAM, I/F card, option circuit board, or CPU circuit board
RESPONSE: Replace RAM, I/F card, option circuit board, or CPU circuit board
EXPLANATION: This error is indicated if a NMI occurs during the first 400µs after NMI is allowed.
A NMI occurs under one of the following conditions:
(1) a RAM parity check error occurs
(2) an I/O channel error occurs.

MESSAGE	PORT(80)
105-System board error	2Ch

NEXT: HALT
CAUSE: 8042 (8742)
RESPONSE: Replace 8042 (8742)
EXPLANATION: The IBF bit in the 8042 (8742) status register was not cleared even after a fixed time elapsed. Checking is performed in the same way as for test 16h.

MESSAGE	PORT(80)
(none)	2Eh,36h, or 3Bh

NEXT: HALT
CAUSE: CPU
RESPONSE: Restart or replace CPU
EXPLANATION: The protection enable (PE) bit in the CPU machine status word (MSW) register was turned on but the bit was off when verified.

MESSAGE	PORT(80)
(none)	31h or 32h

NEXT: HALT
CAUSE:
RESPONSE:
EXPLANATION: An error occurred while checking address lines 19 to 23.
The address lines are checked by writing FFFFh in address 0000:0000. 00h is then written in the following addresses: 0800:0000, 1000:0000, 2000:0000, 4000:0000, and 8000:0000. If the data stored in address 0000:0000 is FFFFh, address lines A19 to A23 are functioning normally.

MESSAGE	PORT(80)
202-Memory address error	38h

NEXT: CONTINUE
CAUSE: RAM
RESPONSE: Replace RAM
EXPLANATION: A bad RAM chip or parity error was detected while checking the RAM size. In either case, an error address and error bit pattern are displayed on the CRT screen.

If a bad RAM is detected the address and bit pattern are displayed as follows:

```
xxxxxx  **** 202-Memory address error
```

xxxxxx is the error address. If an address from 000000h to 07FFFFh is indicated, there is an error in the 256K-bit RAM on the memory board. If an address from 080000h to 09FFFFh is indicated, there is an error in the 64K-bit RAM. If an address from 100000h to FDFFFFh is indicated, there is an error in RAM on an option card.
**** is the error pattern, as explained for test 11h.

For a parity error the error data is shown as follows:

```
xxxxxx  0000 202-Memory address error
```

The error detection address is as described above, but all zeros are displayed for the bit pattern. The next line on the display shows this message:

```
                - Parity check n
```

If n is 1 this indicates a RAM parity error on the memory board, if it is 2 there is a parity error on an optional memory card.

MESSAGE	PORT(80)
203-Memory address error	3Ah

NEXT: CONTINUE
CAUSE:
RESPONSE:
EXPLANATION: A bad RAM or parity error was detected while checking the address lines. The address lines are checked as follows:
(1) data is written in the RAM specified at the start address of the 64K byte block
(2) the data is verified after it has been written in all blocks
(3) an error occurs if any data is not correctly verified.

MESSAGE	PORT(80)
304-Keyboard or System Unit error	3Eh

NEXT: CONTINUE
CAUSE: Keyboard unit or 8042 (8742)
RESPONSE: Replace the keyboard unit or 8042 (8742)
EXPLANATION: The T0 bit (indicating the clock sent from the keyboard) of the test input port in the 8042 (8742) was not turned low.

MESSAGE	PORT(80)
301-Keyboard error 303-Keyboard or System unit error	3Fh

NEXT: CONTINUE
CAUSE: Keyboard unit, 8042 (8742), or CPU circuit board
RESPONSE: Replace keyboard, 8042 (8742), or CPU circuit board
EXPLANATION: If an error is detected during the keyboard unit self-test, a keyboard interface check is performed and the interface line test command is output, to determine whether the error was caused by keyboard failure or by disconnected status. This error is indicated if **NO** error is determined as a result of the keyboard interface check, or if the response to the interface line test command is not returned or indicates an error.

This error is also indicated if a code is being output repeatedly from the keyboard, for example if a key is stuck. In this case, the two-digit hexadecimal key code is displayed on the CRT screen before the error message.

MESSAGE	PORT(80)
401-CRT error 501-CRT error	42h

NEXT: CONTINUE
CAUSE: Monitor-type switch setting
RESPONSE: Set the switch correctly
EXPLANATION: The setting of the monitor-type switch did not match with the installed primary video card.

If 401-CRT error is displayed on the CRT screen, the monochrome monitor was selected by the switch but the video card indicates a color monitor.

If 501-CRT error is displayed on the CRT screen, the color monitor was selected by the switch but the video card indicates a monochrome monitor.

MESSAGE	PORT(80)
161-System options not set	42h

NEXT: CONTINUE
CAUSE: Lithium battery
RESPONSE: Replace the lithium battery
EXPLANATION: RTC power failure was detected. This error is indicated if the VRT bit in the RTC (146818) control register D is 0.

MESSAGE	PORT(80)
162-System options not set	42h

NEXT: CONTINUE
CAUSE: RTC(146818) setting error
RESPONSE: Replace or correctly set RTC (146818)
EXPLANATION: An error occurred in RTC check sum or the RTC contents did not match the installed hardware.

MESSAGE	PORT(80)
164-Memory size error	42h

NEXT: CONTINUE
CAUSE: CMOS setting error
RESPONSE: Perform setting correctly
EXPLANATION: This error is indicated if the amount of installed RAM differs from the value stored in the CMOS RAM on the RTC chip.

MESSAGE	PORT(80)
163-Time & Date Not Set	42h

NEXT: CONTINUE
CAUSE: RTC (146818) or CPU circuit board
RESPONSE: Replace RTC (146818) or the CPU circuit board
EXPLANATION: This error is indicated if the RTC control register was read but processing did not set the update in progress status bit (CMOS OAh bit 7), or the update in progress status bit could not be cleared.

MESSAGE	PORT(80)
601-Diskette error	43h

NEXT: CONTINUE
CAUSE: FDD, SPFG circuit board, WHDC circuit board
RESPONSE:
(1) Replace the faulty FDD.
(2) Install the missing SPFG or WHDC circuit board.
(3) Replace the faulty SPFG or WHDC circuit board.
EXPLANATION:
(1) An error was returned when the FDC was reset (INT 13h, AH=0; reset function).
(2) The FDD was reset normally as a result of the above check, but an error was returned during the head seek test only drive A is checked.
(3) A card equivalent to the IBM combination controller card did not exist, ie. the SPFG or WHDC circuit board is missing.

MESSAGE	PORT(80)
1780-Disk 0 failure 1781-Disk 1 failure	45h

NEXT: CONTINUE
CAUSE: HDD, WHDC circuit board
RESPONSE: Replace the HDD or WHDC circuit board
EXPLANATION: The hard disk could not be recalibrated.

If 1780 – Disk 0 failure is displayed on the CRT screen, the CMOS data in the RTC is rewritten and IPL from the HDD is disabled.

MESSAGE	PORT(80)
1782-disk controller failure	45h

NEXT: CONTINUE
CAUSE: WHDC circuit board
RESPONSE: Replace the WHDC circuit board
EXPLANATION: An abnormal code was returned during the hard-disk controller self-test.

MESSAGE	PORT(80)
1790-Disk 0 error 1791-Disk 1 error	45h

NEXT: CONTINUE
CAUSE: CMOS setting error
RESPONSE: Perform setting correctly
EXPLANATION: The maximum cylinder, head, and sector values in the RTC CMOS differ from the ones in the installed hard disk.

MESSAGE	PORT(80)
163-Time & Date Not Set	49h

NEXT: CONTINUE
CAUSE: RTC (146818) or CPU circuit board
RESPONSE: Execute SETUP; replace RTC (146818) or CPU circuit board
EXPLANATION: An out of range error occurred when hour, minutes, and seconds were read even though:
- power was normal
- there was no error in the RTC check sum
- the RTC could set the update in progress status bit correctly
- the RTC could clear the update in progress status bit correctly.

An out of range error occurs in hours, minutes, or seconds as follows:
- hours > 23
- minutes > 59
- seconds > 59.

MESSAGE	PORT(80)
302-System unit keylock is locked	4Ch

NEXT: CONTINUE
CAUSE: This test should never fail
RESPONSE:
EXPLANATION: This test is provided for computers that have a system unit keylock. This machine does not have a keylock, and the keyboard locked status is always set to unlocked.

4.3 ADVANCED TROUBLESHOOTING

This section describes advanced troubleshooting techniques for the EPSON PC AX2.

4.3.1 OPERATING GUIDE FOR THE ANDRO MAIN BOARD TEST PROGRAM

This test program is supplied as two pairs of ROM chips; one pair one is used to output the test results to a parallel interface device and the other is used to output the results to a serial interface device. Choose which pair of chips will be used (depending on the output device to be used, i.e. serial printer or parallel printer). Carefully remove the ROM BIOS chips from the System Memory Board and place them aside. The test ROM chips must then be installed in sockets 3B (odd address ROM) and 4B (even address ROM).

It is possible to monitor the test results with the LED displays on the MFG2 board installed in an expansion slot. Each individual test item is selected by setting the DIP switches on the MFG2 board. The program tests each of the operating functions required to boot the system up.

4.3.2 TOOLS REQUIRED

TABLE 4-3. TOOLS REQUIRED

PARALLEL I/F OUTPUT	SERIAL I/F OUTPUT (*1)
Test program ROM for parallel I/F output	Test program ROM for serial I/F output
Printer with a parallel interface	Printer or computer with a serial interface
Connecting Cable	Connecting Cable
MFG2 board (*2)	
Oscilloscope or Logic Analizer (*2)	

(*1) Serial interface specifications: DTE typed, 4800 bps, 8 bit, non-parity, 1 stop bit.

(*2) It is possible to execute this test program even if these tools are not available.

4.3.3 DIP SWITCH SETTINGS

Each of the three DIP switches on the MFG2 board should be set as follows:

(1) DIP SW1 AND SW2 (I/O PORT ADDRESS SETTINGS)

DIP switches SW1 and SW2 are use to assign the I/O port address for DIP SW3 and LED1 – LED8, and for specifying whether the DIP SW status is monitored or not.

TABLE 4 – 4. MFG2 BOARD DIP SW1 AND SW2 SETTINGS

ADDRESS (HEX)	SW 2 8 7 6 5 4 3 2 1	SW1 4 3 2 1	FUNCTION
7F0	0 1 1 1 1 1 1 1 (*1)	0 0 0 0	Displays the test item number (*2)
7F1	0 1 1 1 1 1 1 1	0 0 0 1	Displays SW3 status on MFG2 board (*3)
7F3	0 1 1 1 1 1 1 1	0 0 1 1	Monitor the test status
FF0	1 1 1 1 1 1 1 1	0 0 0 0	Test for the MFG2 board

(*1) ON = 0 = "LOW", OFF = 1 = "HIGH"
(*2) LED8 = MSB, LED1 = LSB
(*3) LED8 = SW3-8, LED1 = SW3-1

(2) DIP SW3 (TEST FUNCTION SETTINGS)

DIP switch 3 (SW3) on the MFG2 board is assigned as follows:

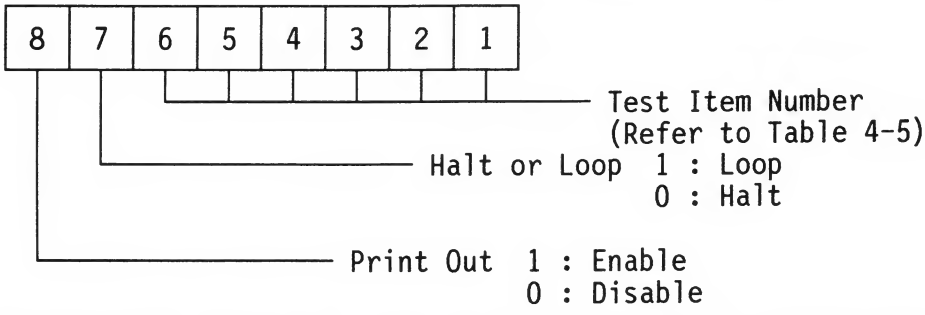


FIGURE 4 – 3. DIP SW 3 ASSIGNMENT

4.3.4 DIAGNOSTICS

The test ROM checks the main circuit board or the MFG2 board, depending on the I/O port address set by SW1 and SW2.

MFG2 BOARD TEST

The status of SW3 on the MFG2 board can be read from the LED indicators on the MFG2 board by setting SW1 and SW2 to FF0H, and then resetting the computer (turn the power switch off/on or push the reset button). The status of the individual switches in SW3 is read from the LEDs: If the LED is OFF, the switch is ON (and if the LED is ON, the switch is OFF). SW3-1 is assigned as the least significant bit (LSB). To finish the test, turn the power switch off or change the I/O address to 7FXH then push the reset button.

TABLE 4-5. DIP SW 3 FUNCTIONS

DIP SW 3 8 7 6 5 4 3 2 1	FUNCTION 0 : Switch On 1 : Switch Off
x x 0 0 0 0 0 0	MFG2 Board Reset, Mask of Int., NMI, CRT Display
x x 0 0 0 0 0 1	CPU Register check
x x 0 0 0 0 1 0	Data Output Port Setup, Hardware Reset
x x 0 0 0 0 1 1	Print Out Opening Message
x x 0 0 0 1 0 0	ROM check sum
x x 0 0 0 1 0 1	8254 (in T4758) #0,1,2 Frequency Test (1kHz)
x x 0 0 0 1 1 0	8254 (in T4758) Counter #2 Test (Beep 1kHz)
x x 0 0 0 1 1 1	Set up 8254 (in T4758) Counter #1 for Refresh
x x 0 0 1 0 0 0	8237 (in T4758) Register R/W Test
x x 0 0 1 0 0 1	8237 (in T4758) Page Register R/W Test
x x 0 0 1 0 1 0	8042 Keyboard Interface Test (Self-test)
x x 0 0 1 0 1 1	DRAM R/W test (First 128KB)
x x 0 0 1 1 0 0	DRAM R/W test (Last 512KB)
x x 0 0 1 1 0 1	DRAM R/W test (640KB)
x x 0 0 1 1 1 0	DRAM R/W and Refresh Test
x x 0 0 1 1 1 1	RTC Back-up Power Sense Check
x x 0 1 0 0 0 0	RTC (146818) Backup Test (CMOS RAM Write)
x x 0 1 0 0 0 1	RTC (146818) Backup Test (Read & Write New Data)
x x 0 1 0 0 1 0	RTC (146818) Backup Test (Read data)
x x 0 1 0 0 1 1	RTC (146818) Read/Write Test
x x 0 1 0 1 0 0	8254 (in T4758) Counter #0 Test
x x 0 1 0 1 0 1	8259 (in T4758) Setup
x x 0 1 0 1 1 0	Interrupt Test (INT0)
x x 0 1 0 1 1 1	Keyboard Test (INT1), Keyboard Print Out
x x 0 1 1 0 0 0	FDD Motor Test
x x 0 1 1 0 0 1	Release FDC reset and FDD recalibrate test
x x 0 1 1 0 1 0	FDD seek test
x x 0 1 1 0 1 1	FDD read test and load boot program (TK00, sec0)
x x 0 1 1 1 0 0	Read, load and print out dump list
x x 0 1 1 1 0 1	Read, load and jump to boot program
x x 0 1 1 1 1 0	Read, load, dump and jump
x x 0 1 1 1 1 1	Read, load, jump and another disk
x x 1 0 0 0 0 0	Read, load, dump, jump and another disk
x x 1 1 0 0 0 0	Repeat function 02-09, 0E, 0F, 13-1B
x x 1 1 0 0 0 1	Repeat Function 30 - Boot Program Load

Execution Process by DIP SW3 on the main control board

TABLE 4-6. EXECUTION PROCESS BY DIP SW3 SETTINGS - I

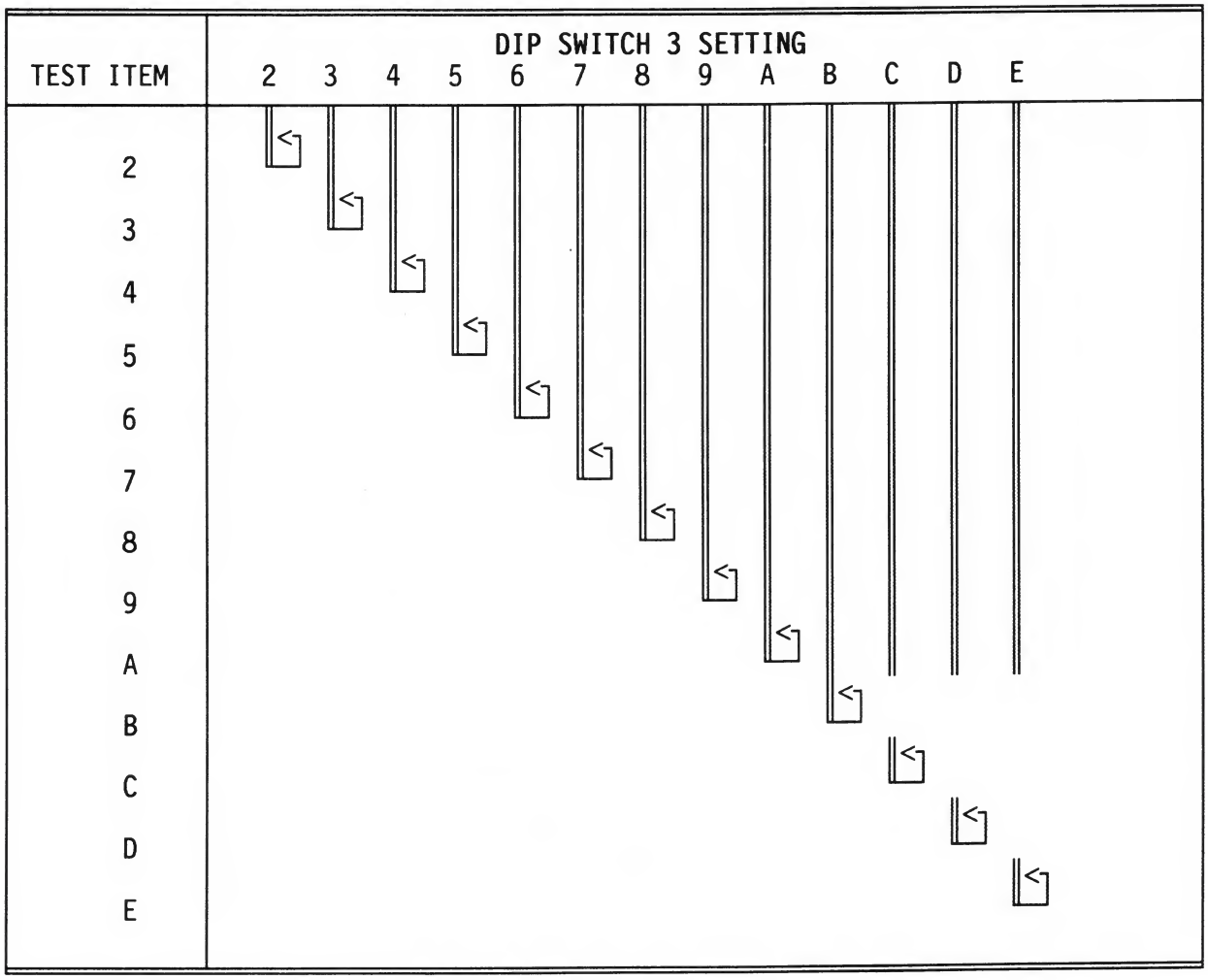


TABLE 4-7. EXECUTION PROCESS BY DIP SW SETTINGS - II

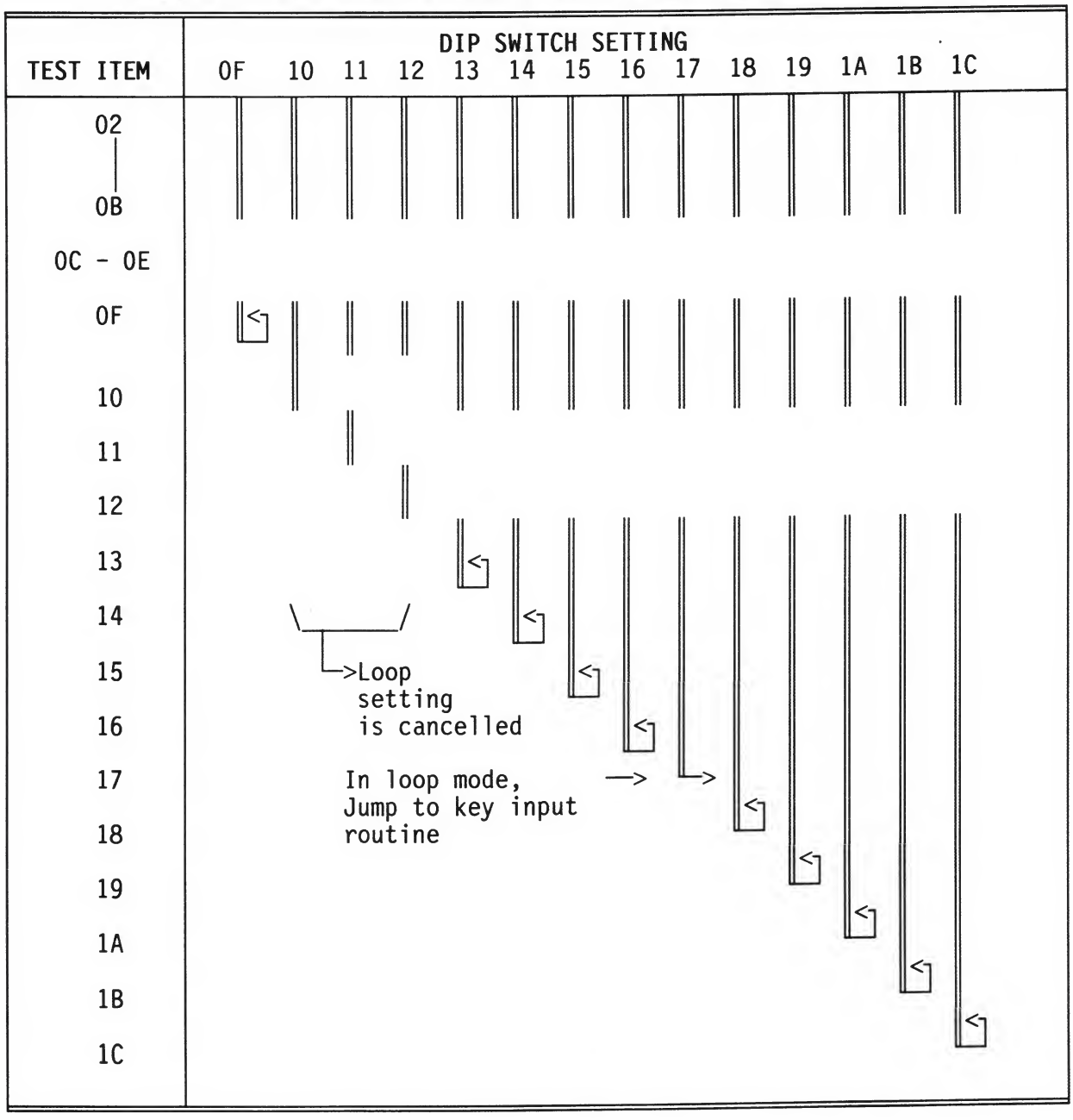
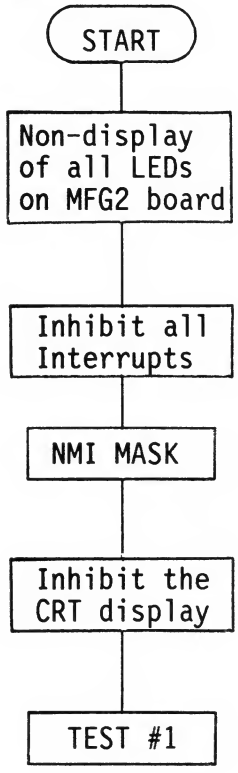


TABLE 4-8. EXECUTION PROCESS BY DIP SW SETTINGS - III

TEST ITEM	DIP SWITCH SETTING 1D	1E	1F	20	30	31
02						
03						
04						
05						
06						
07						
08						
09						
0A						
0B						
0C						
0D						
0E						
0F						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
1A						
1B						
1C						
1D						
1E						
1F						
20						
30						
31						

TEST ITEM # 0	TEST : MFG2 BOARD RESET, MASK OF INT,NMI, CRT DISPLAY

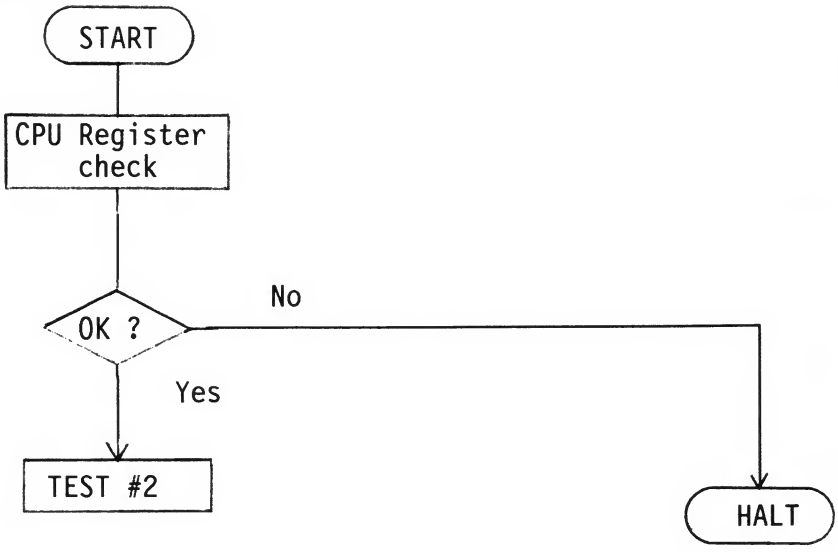
(DESCRIPTION)



(REFER TO)

TEST ITEM # 1	TEST : CPU REGISTER CHECK

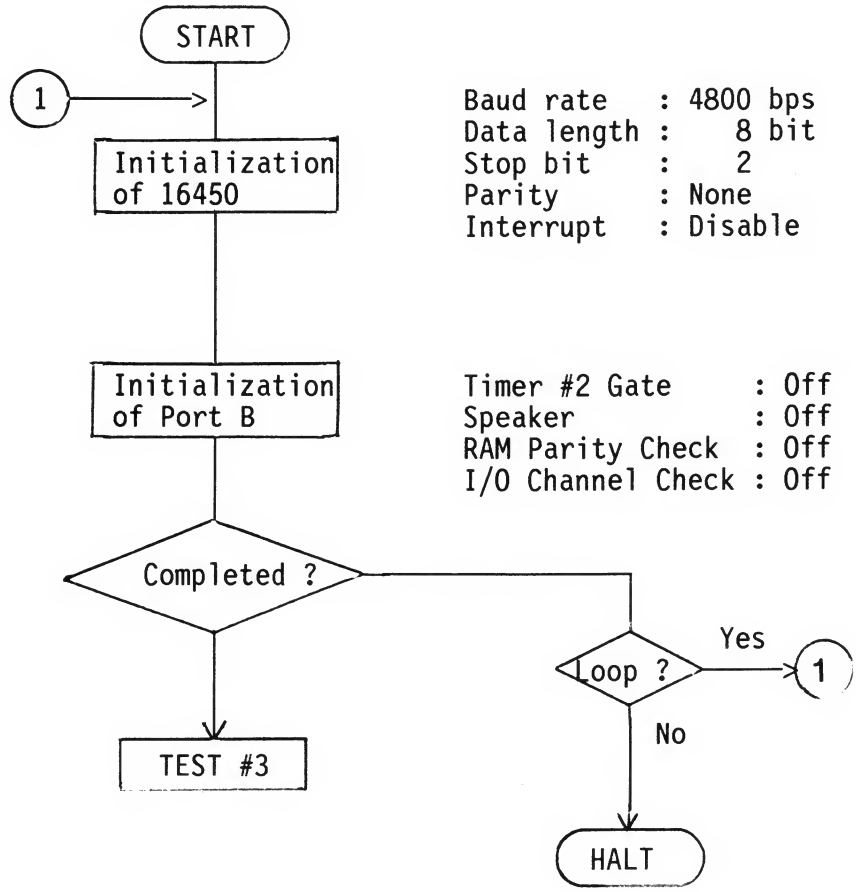
(DESCRIPTION)



(REFER TO)

TEST ITEM # 2	TEST : DATA OUTPUT PORT SETUP, HARDWARE RESET

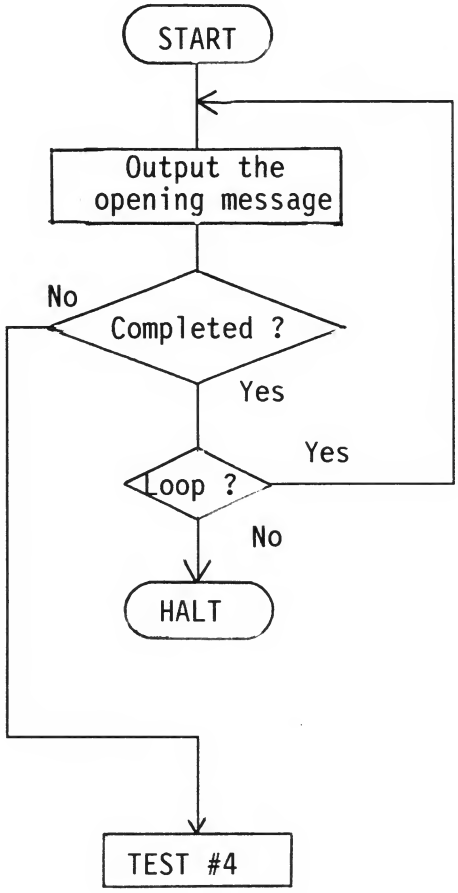
(DESCRIPTION)



(REFER TO)

TEST ITEM # 3	TEST : PRINT OUT THE OPENING MESSAGE

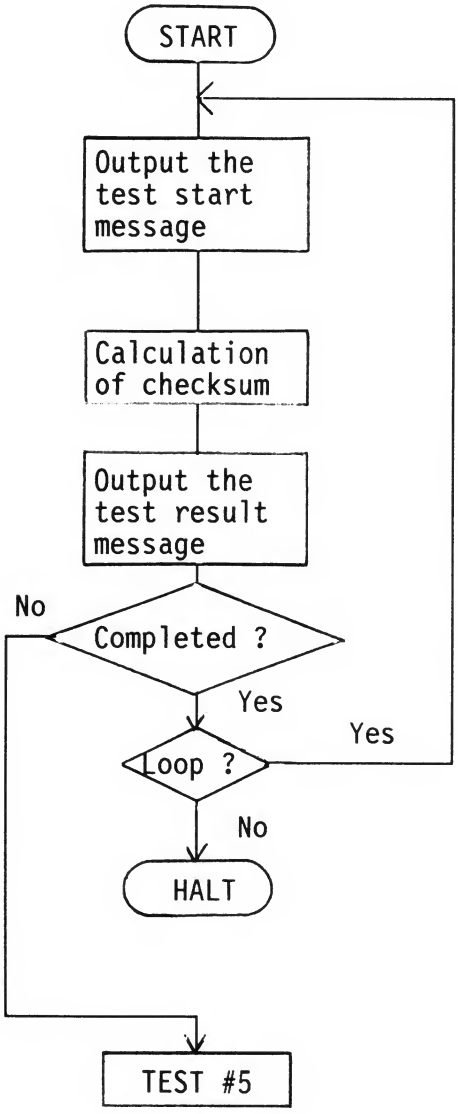
(DESCRIPTION)



(REFER TO)

TEST ITEM # 4	TEST : ROM CHECKSUM TEST

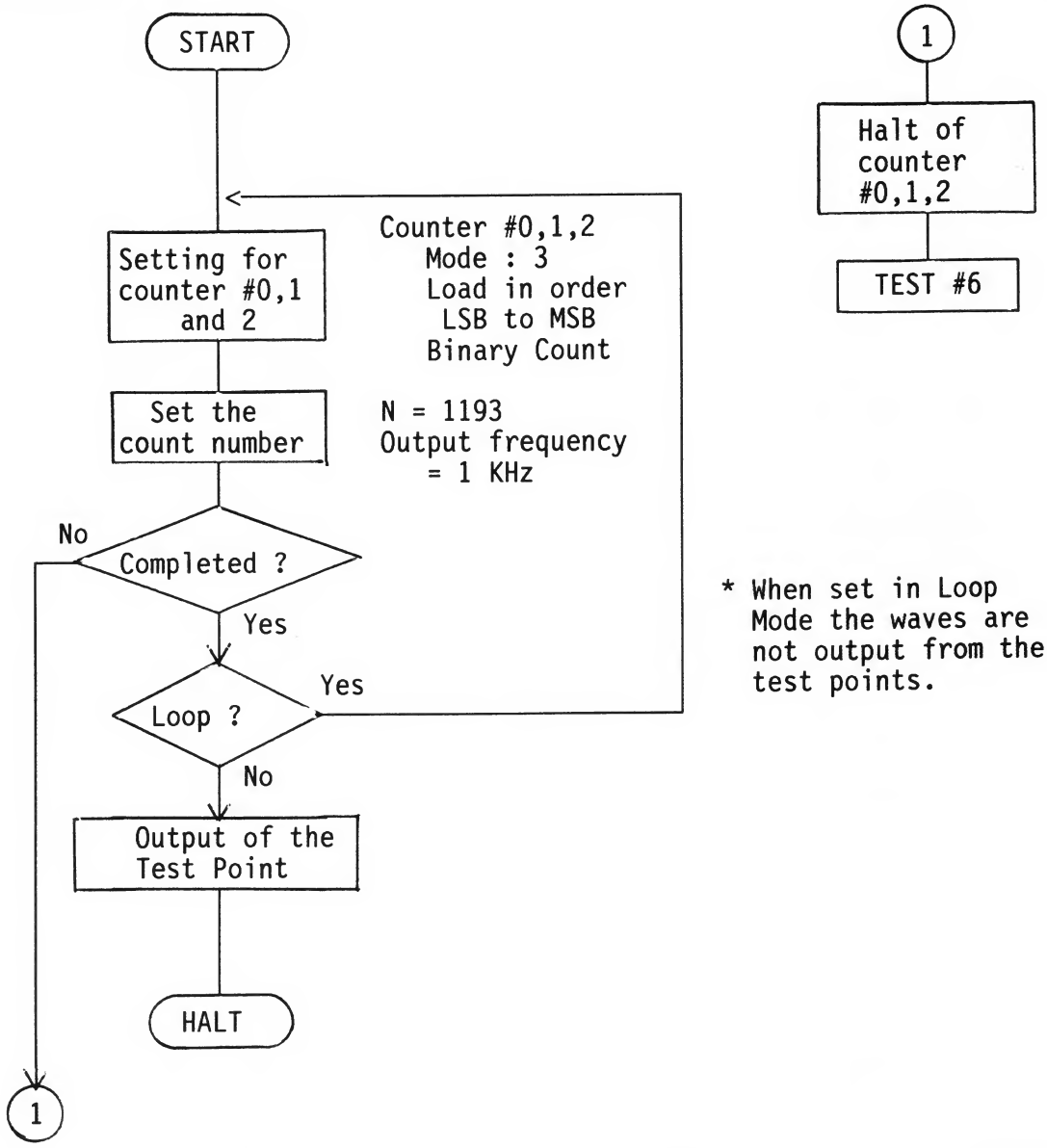
(DESCRIPTION)



(REFER TO)

TEST ITEM # 5	TEST : 8254 (in T4758) #0,1,2 Frequency Test (1KHz)

(DESCRIPTION)



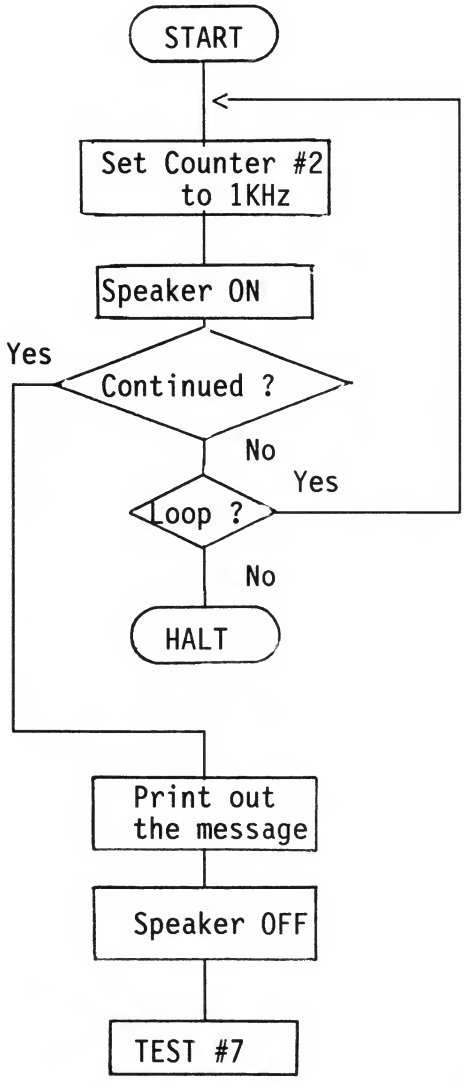
(REFER TO)

STATUS	TEST POINT	REFERENCE (*)
HALT	T4758 (1B) Pin 22, 23 (#0, #1)	WAVEFORM - 1
	T4758 (1B) Pin 24 (#2)	WAVEFORM - 2

*) Waveforms are shown after page 4- 58 .

TEST ITEM # 6	TEST : 8254 (in T4758) Counter #2 Test (Beep 1KHz)

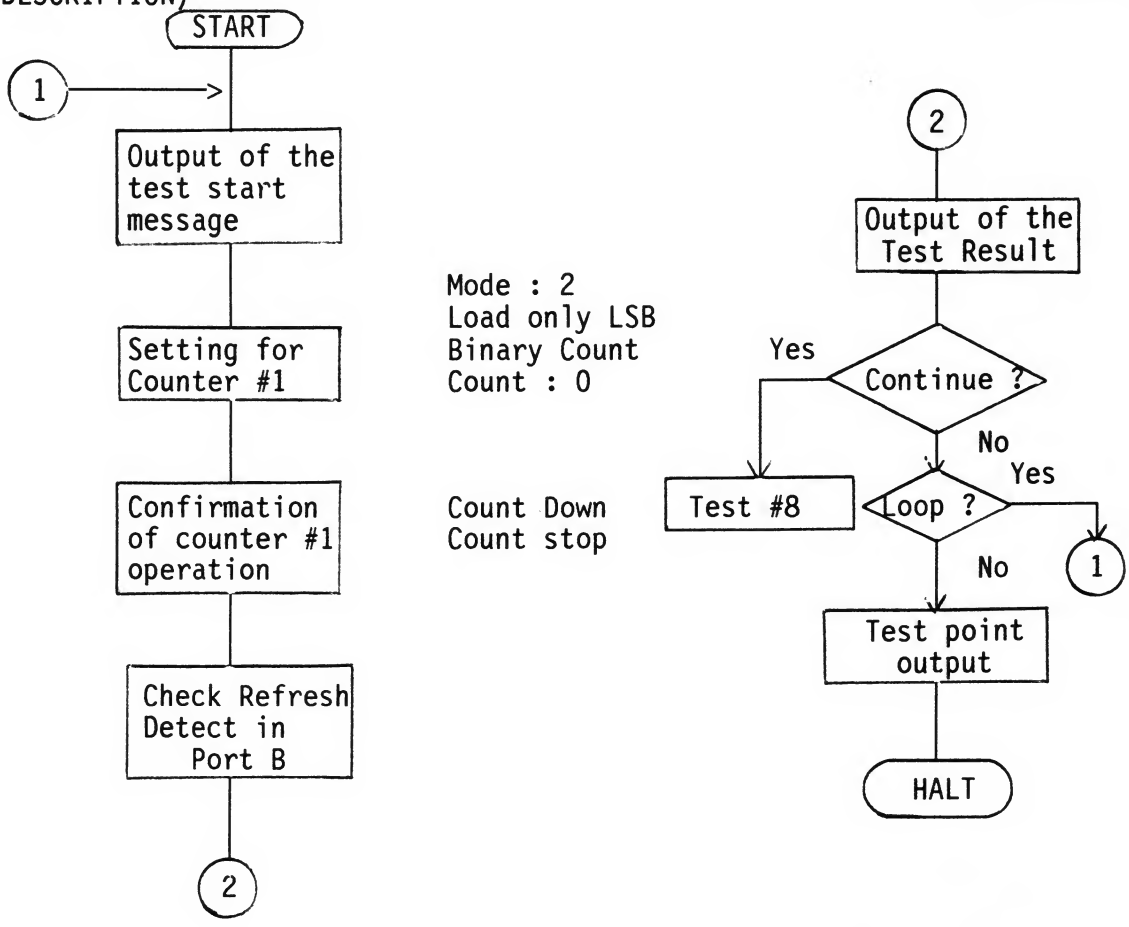
(DESCRIPTION)



(REFER TO)

TEST ITEM # 7	TEST : 8254 (in T4758) Counter #1 Refresh Test

(DESCRIPTION)



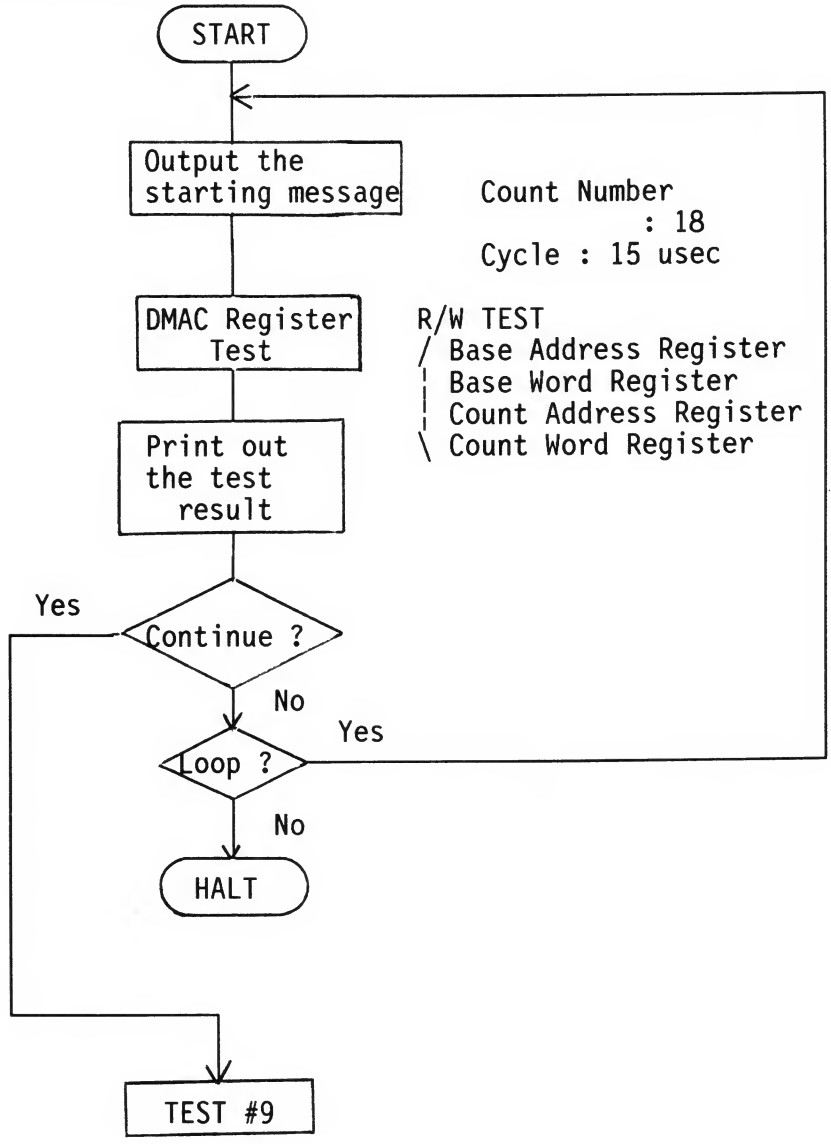
(REFER TO)

STATUS	TEST POINT	REFERENCE
HALT	T4758 (1B) Pin 23 (OUT1)	WAVEFORM - 3
	GAATRF (6D) Pin 63, 28	- 4
	GAATRF (6D) Pin 28, GAATIO (3C) Pin 85	- 5
	GAATM2 ( ) Pin 59, 60	- 6

WAVEFORM 7 through 14 ..... Address line waveform at refresh
WAVEFORM 15 ..... A0 - A7 signals restored with the leading edge of the DRAM RAS signal as an external clock.

TEST ITEM # 8	TEST : 8237 (in T4758) REGISTER R/W TEST

(DESCRIPTION)

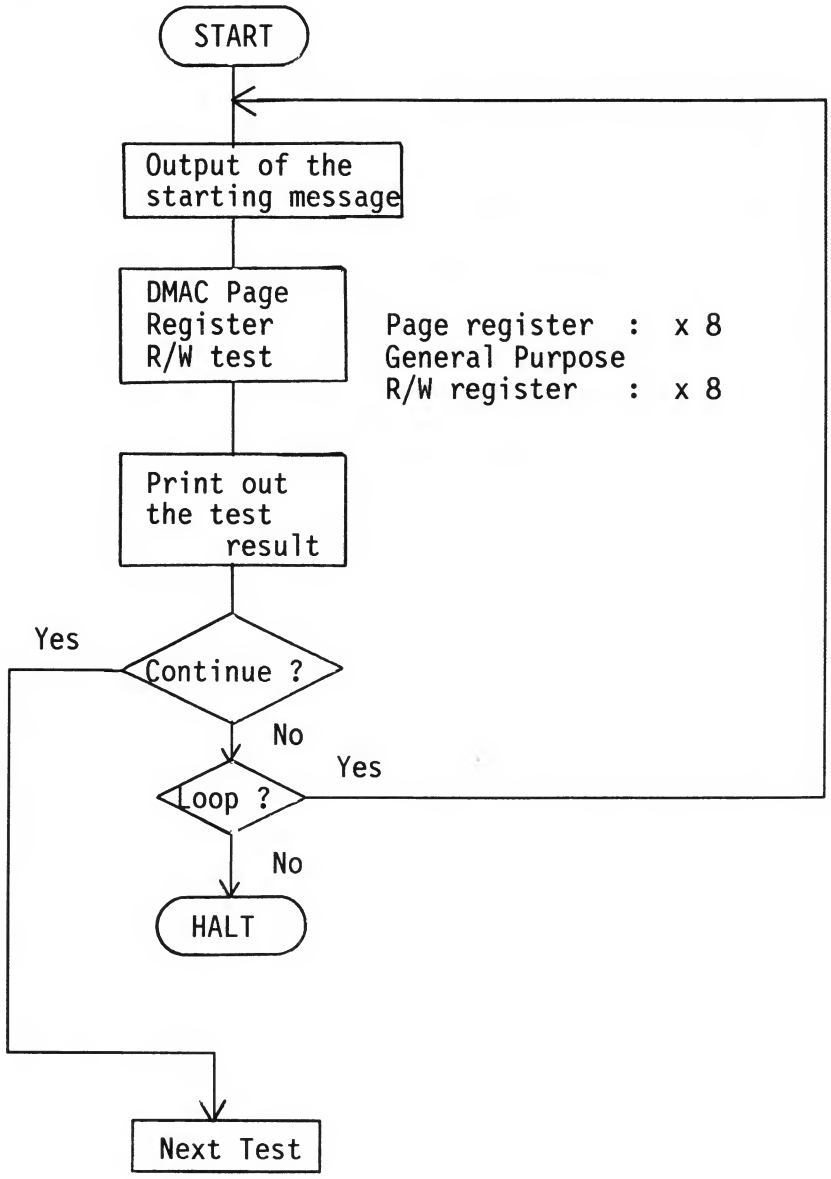


(REFER TO)

STATUS	TEST POINT	REFERENCE
HALT	T4750 (4F) Pin 58	WAVEFORM - 3

TEST ITEM # 9	TEST : 8237 (in T4758) PAGE REGISTER R/W TEST

(DESCRIPTION)

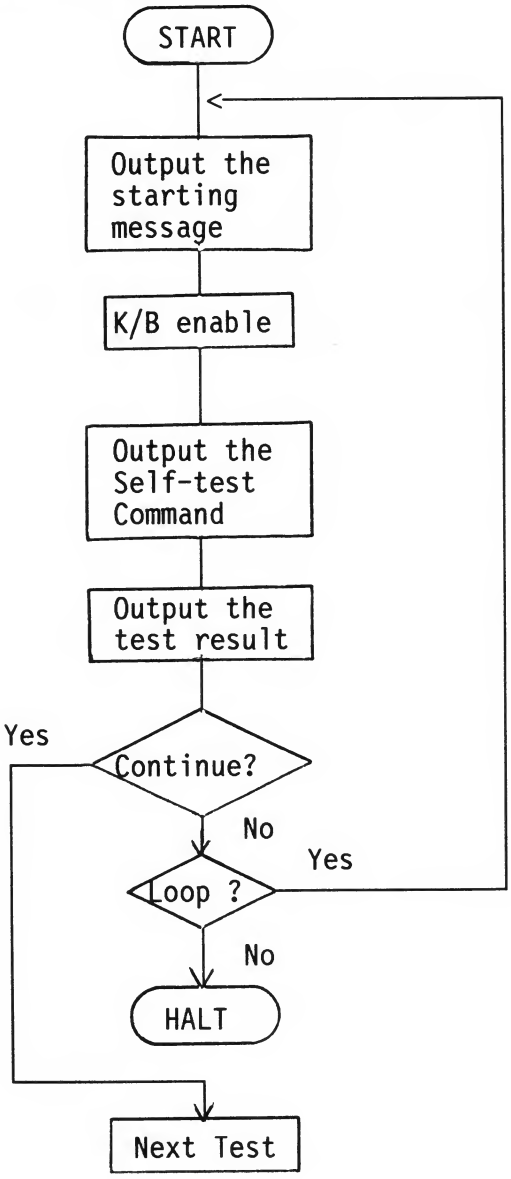


(REFER TO)

STATUS	TEST POINT	REFERENCE
HALT	T4750 (4F) Pin 58	WAVEFORM - 3

TEST ITEM # A	TEST : 8042 KEYBOARD INTERFACE TEST (SELF-TEST)

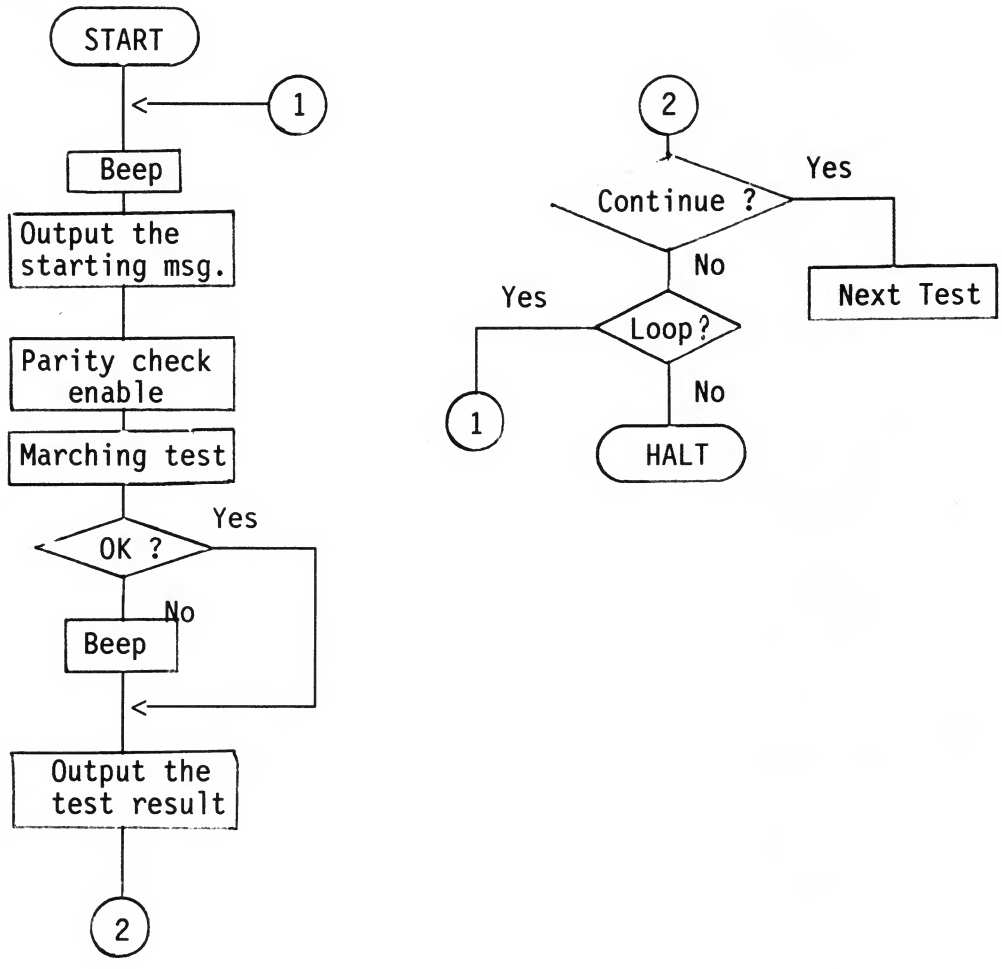
(DESCRIPTION)



(REFER TO)

TEST ITEM # B	TEST : DRAM R/W TEST (FIRST 512KB)

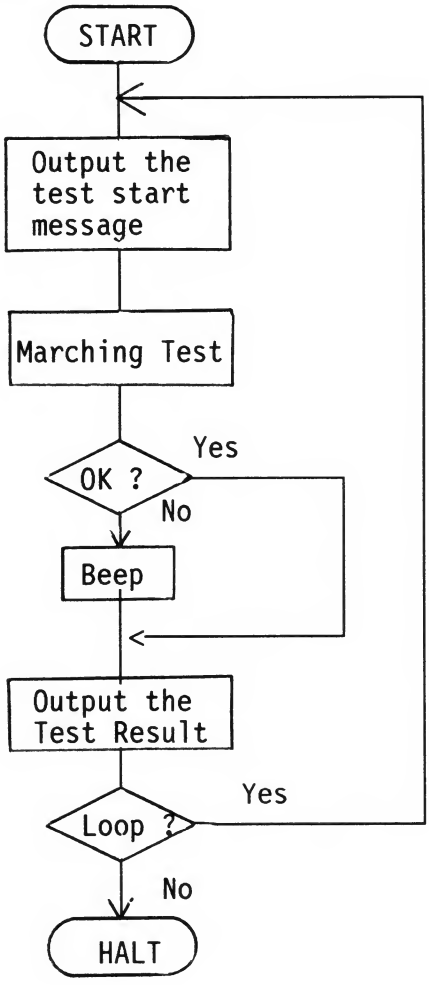
(DESCRIPTION)



(REFER TO)

TEST ITEM # C	TEST : DRAM R/W TEST (LAST 128KB)

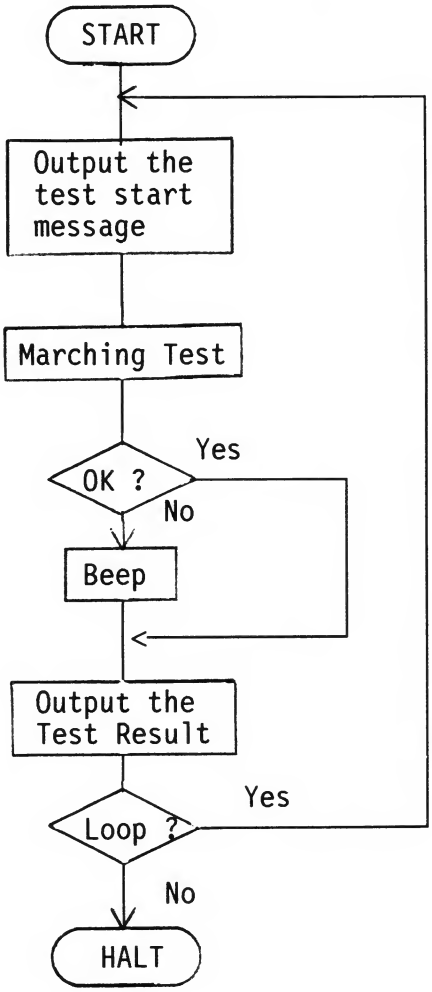
(DESCRIPTION)



(REFER TO)

TEST ITEM # D	TEST : DRAM R/W TEST (640KB)

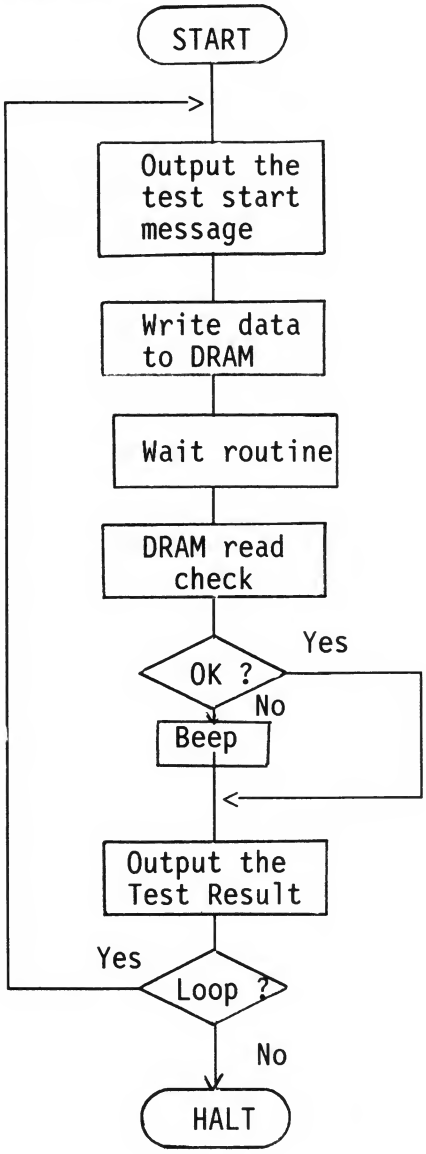
(DESCRIPTION)



(REFER TO)

TEST ITEM # E	TEST : DRAM R/W AND REFRESH TEST

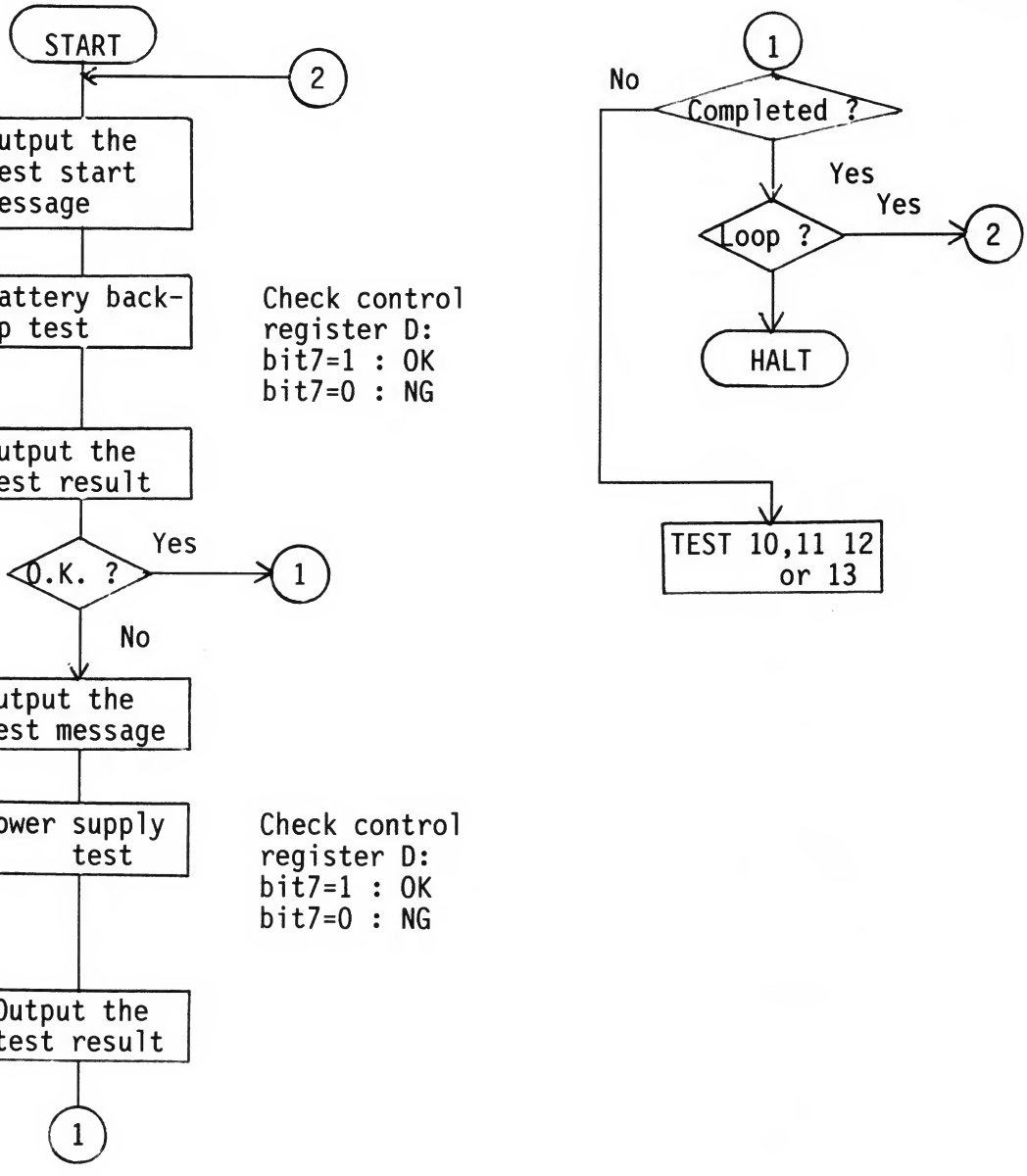
(DESCRIPTION)



(REFER TO)

TEST ITEM # F	TEST : RTC BATTERY BACKUP POWER SENSE TEST

(DESCRIPTION)

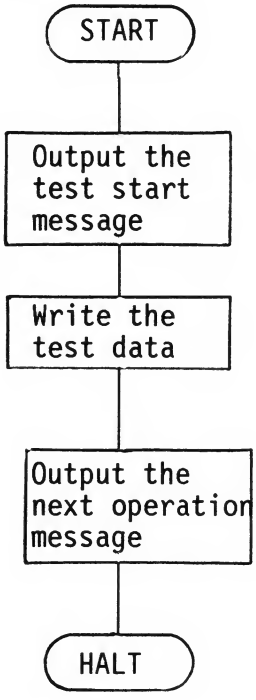


(REFER TO)

Bit 7 of control register D is used for the battery backup test.
When reading the control register, bit 7 is set to 1.
If bit 7 is 0 when this register is read the second time, it means that the RTC is not receiving power correctly or that the RTC is not functioning correctly.

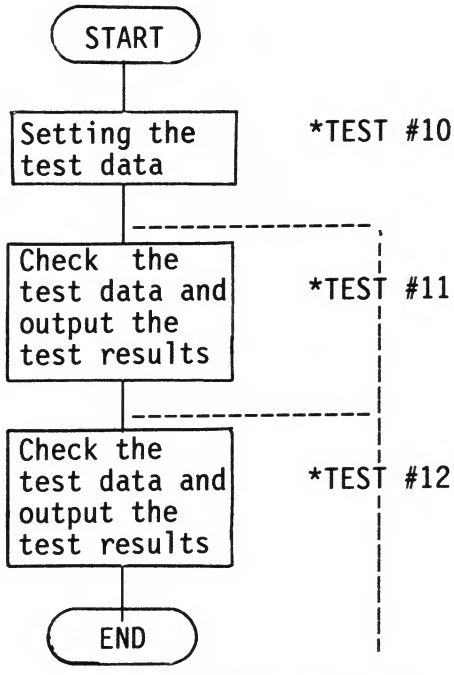
TEST ITEM # 10	TEST : RTC BACKUP TEST (CMOS RAM WRITE)

(DESCRIPTION)



TEST DATA
: 55H

* Test items #10 through #12 are for SRAM backup test in RTC. The test flow chart is shown below.

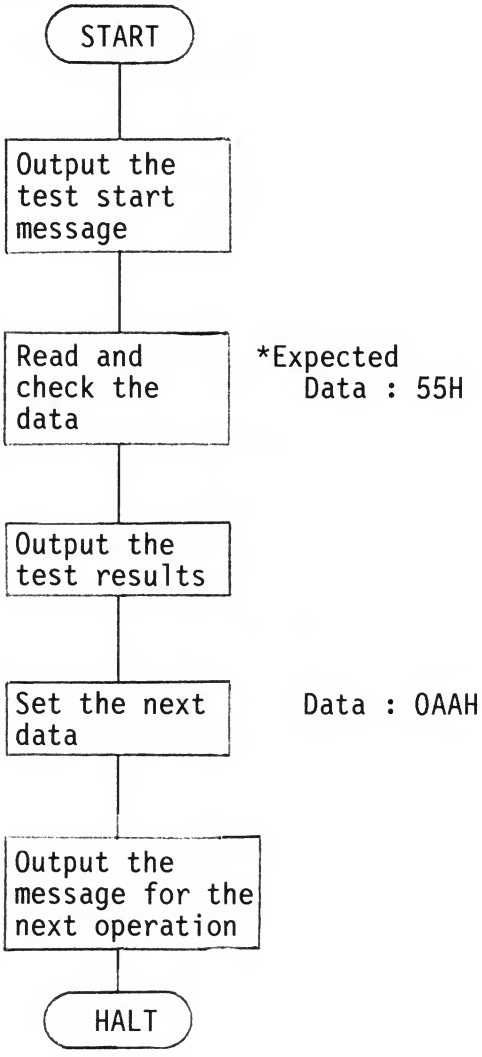


*Turn the power off, set the DIP SW again, then power on a few minutes later.

(REFER TO)

TEST ITEM # 11	TEST : RTC BACKUP TEST (READ & WRITE NEW DATA)

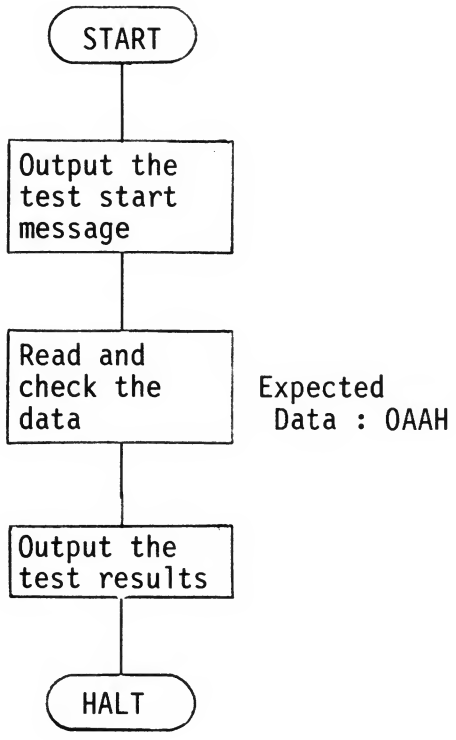
(DESCRIPTION)



(REFER TO)

TEST ITEM # 12	TEST : RTC BACKUP TEST (CMOS RAM READ)

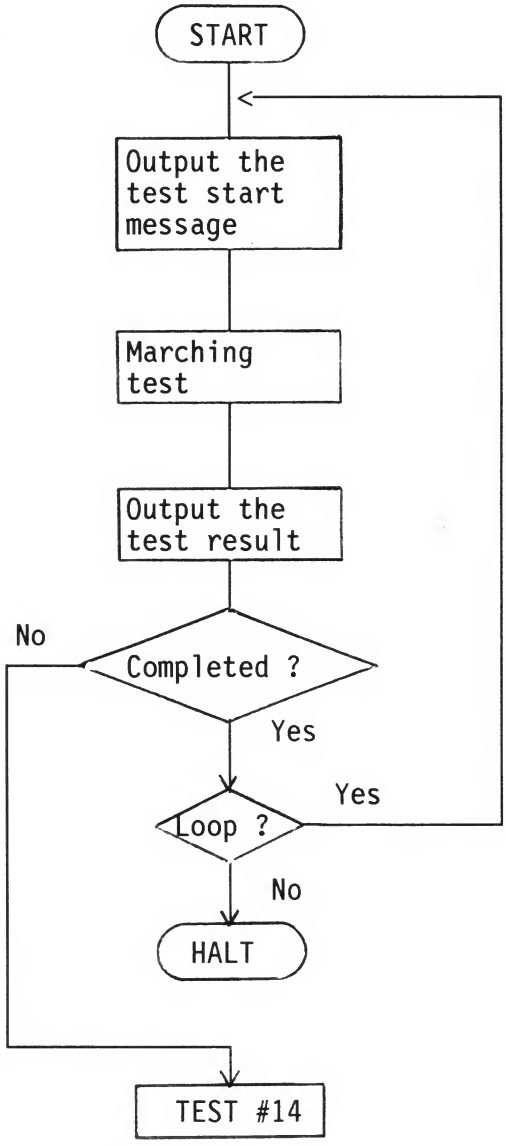
(DESCRIPTION)



(REFER TO)

TEST ITEM # 13	TEST : RTC CMOS RAM R/W TEST

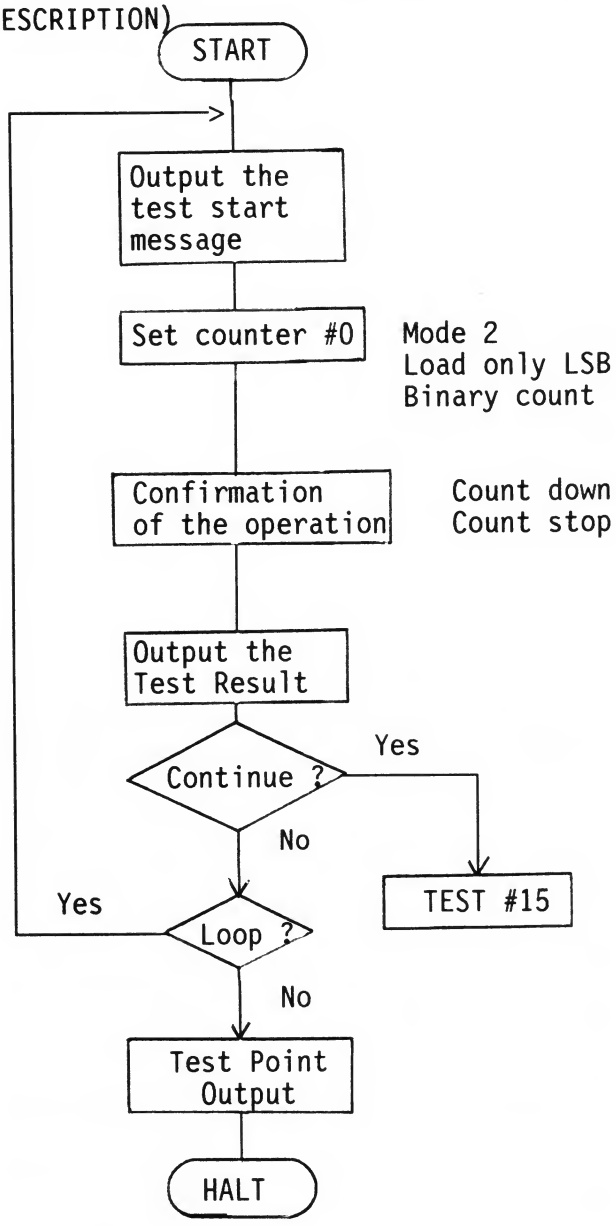
(DESCRIPTION)



(REFER TO)

TEST ITEM # 14	TEST : 8254 COUNTER #0 TEST

(DESCRIPTION)

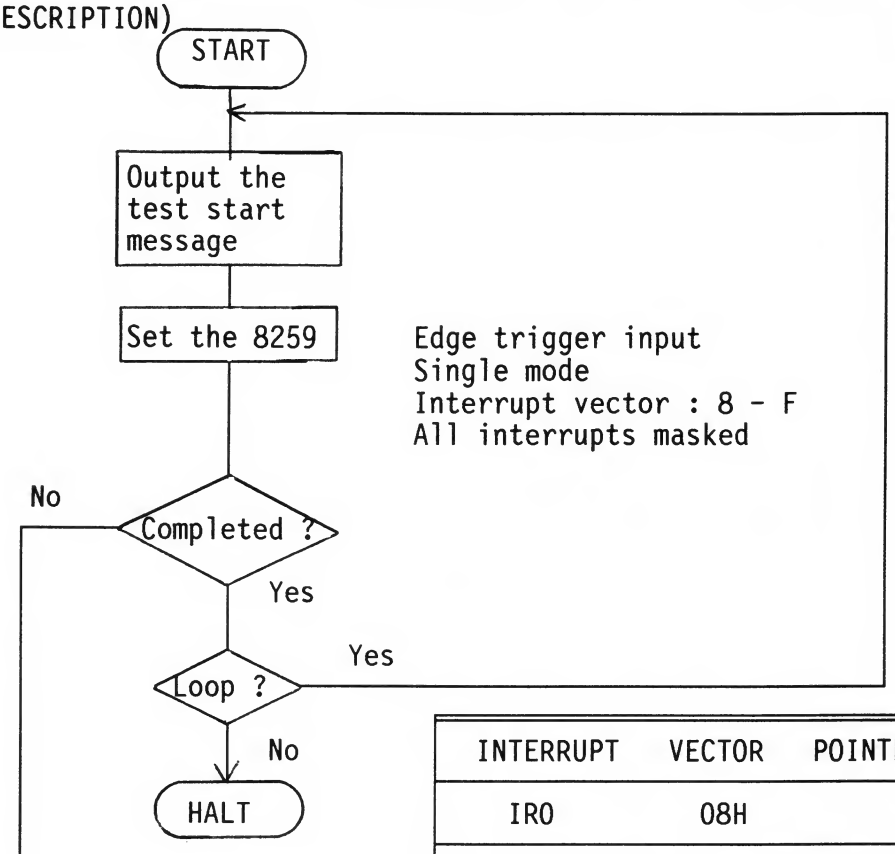


(REFER TO)

STATUS	TEST POINT	REFERENCE
HALT	T4758 (1B) Pin 22 (#0)	WAVEFORM - 16

TEST ITEM # 15	TEST : Setting of the 8259

(DESCRIPTION)

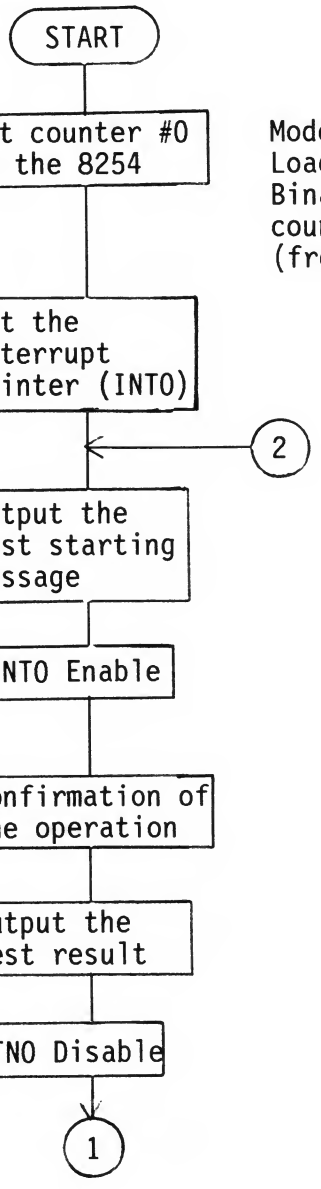


INTERRUPT	VECTOR	POINTER HEAD ADDRESS
IR0	08H	20H
IR1	09H	24H
IR2	0AH	28H
IR3	0BH	2CH
IR4	0CH	30H
IR5	0DH	34H
IR6	0EH	38H
IR7	0FH	3CH

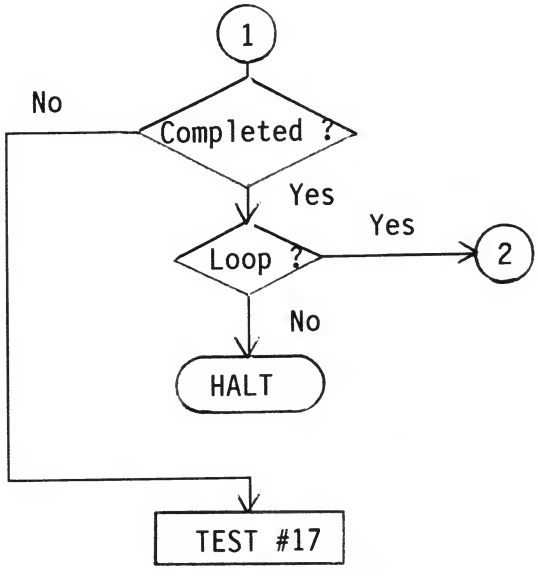
(REFER TO)

TEST ITEM # 16	TEST : INTERRUPT TEST (INTO)

(DESCRIPTION)



Mode 3
Load as order LSB to MSB
Binary count
count number = 11900
(frequency = 100 Hz)



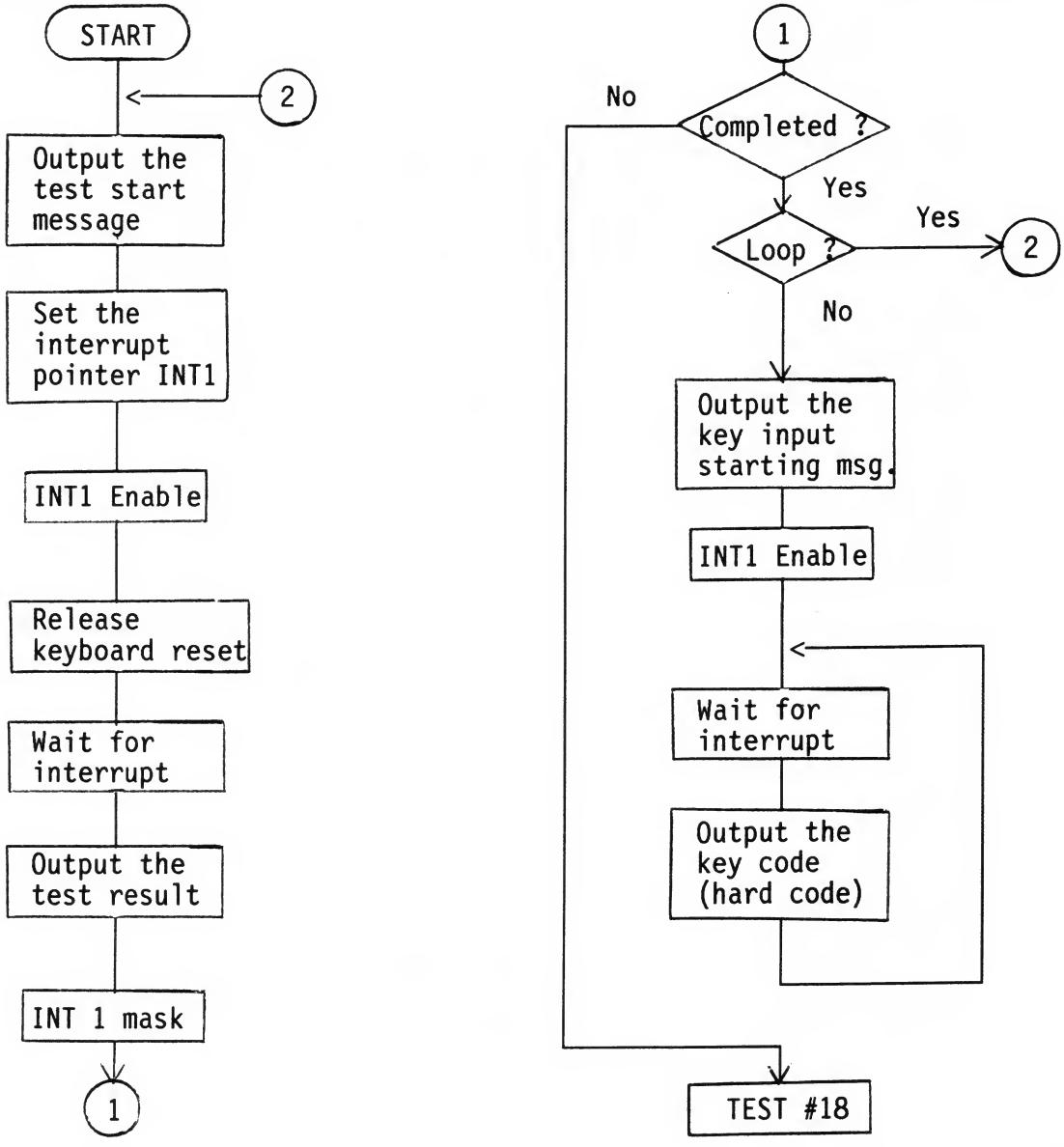
If an interrupt occurs after the release of the interrupt, the operation should be normal.

(REFER TO)

WAVEFORM 17 .... OUT0 and INT0
WAVEFORM 18 .... INT0 and INTA
WAVEFORM 19 .... Signal waveforms at an interrupt mode.

TEST ITEM # 17	TEST : KEYBOARD TEST (INT1), KEYCODE PRINT OUT

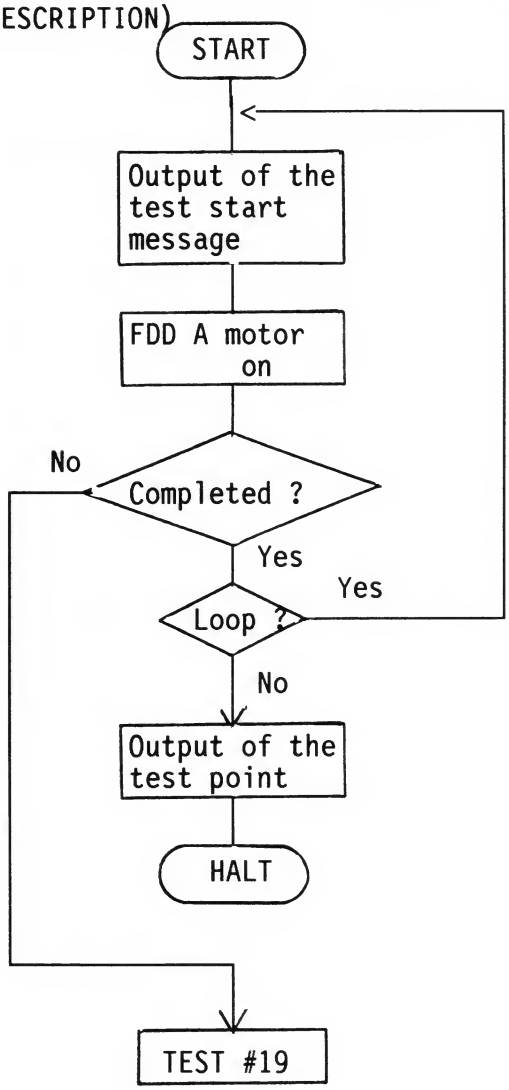
(DESCRIPTION)



(REFER TO)

TEST ITEM # 18	TEST : FDD MOTOR ON

(DESCRIPTION)

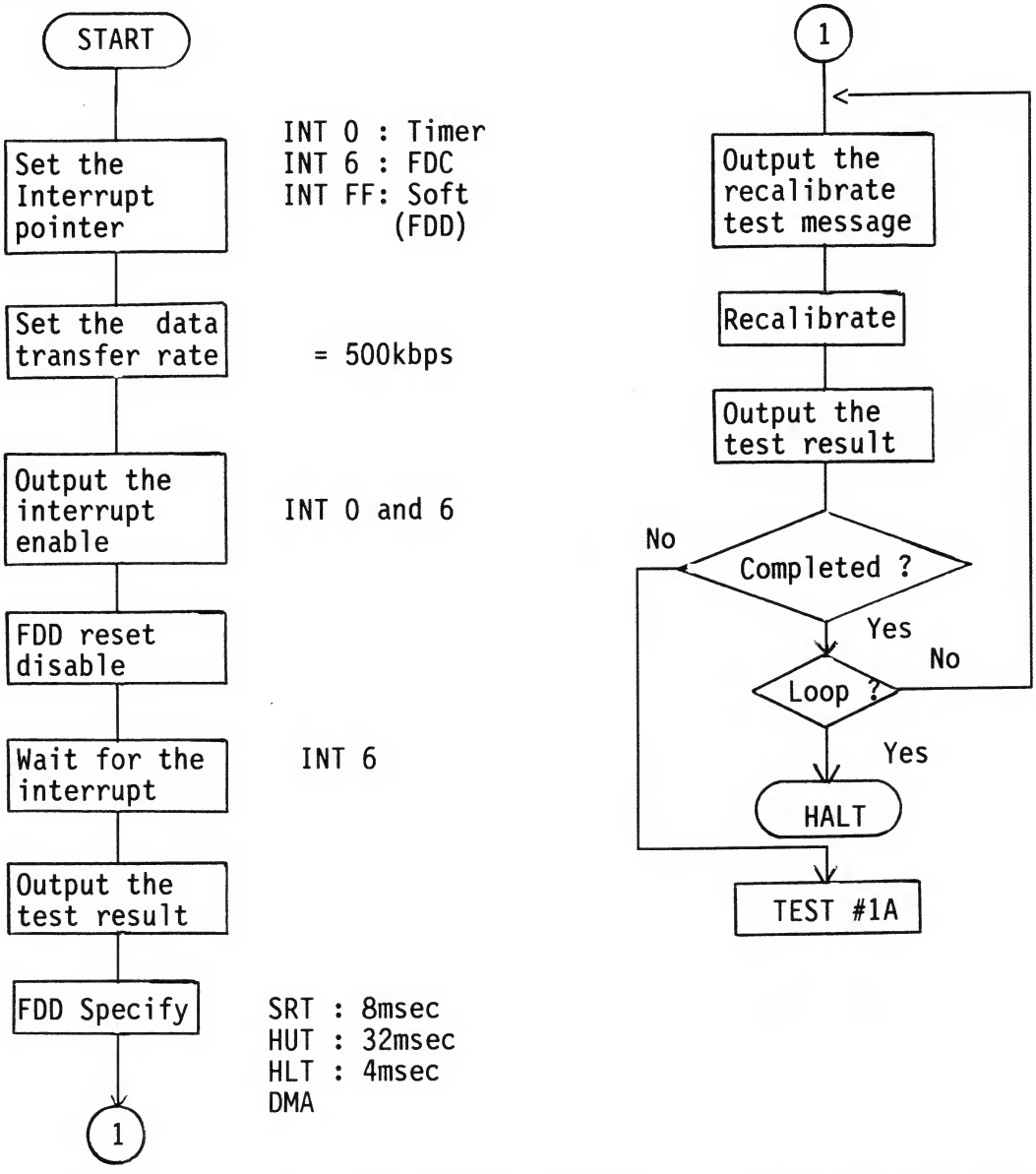


(REFER TO)

STATUS	TEST POINT	REFERENCE
HALT	WD37C65 (1B) Pin 23	WAVEFORM - 20
	WD37C65 (1B) Pin 21	WAVEFORM - 21
	WD37C65 (1B) Pin 39	WAVEFORM - 22

TEST ITEM # 19	TEST : FDC RESET DISABLE & RECALIBRATE TEST

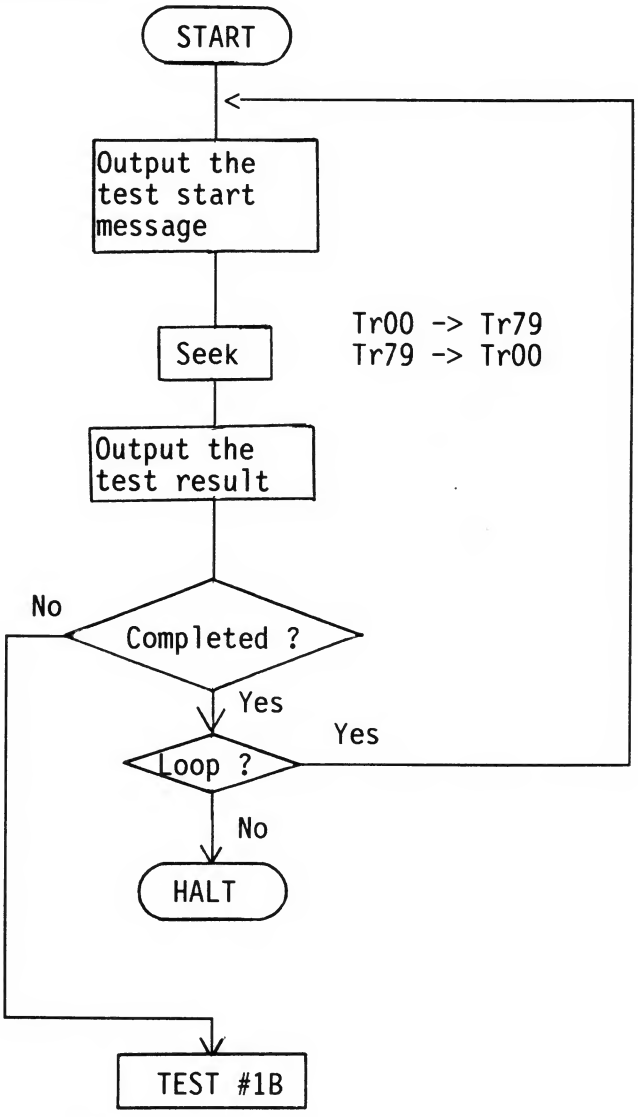
(DESCRIPTION)



(REFER TO)

TEST ITEM # 1A	TEST : FDD SEEK TEST

(DESCRIPTION)



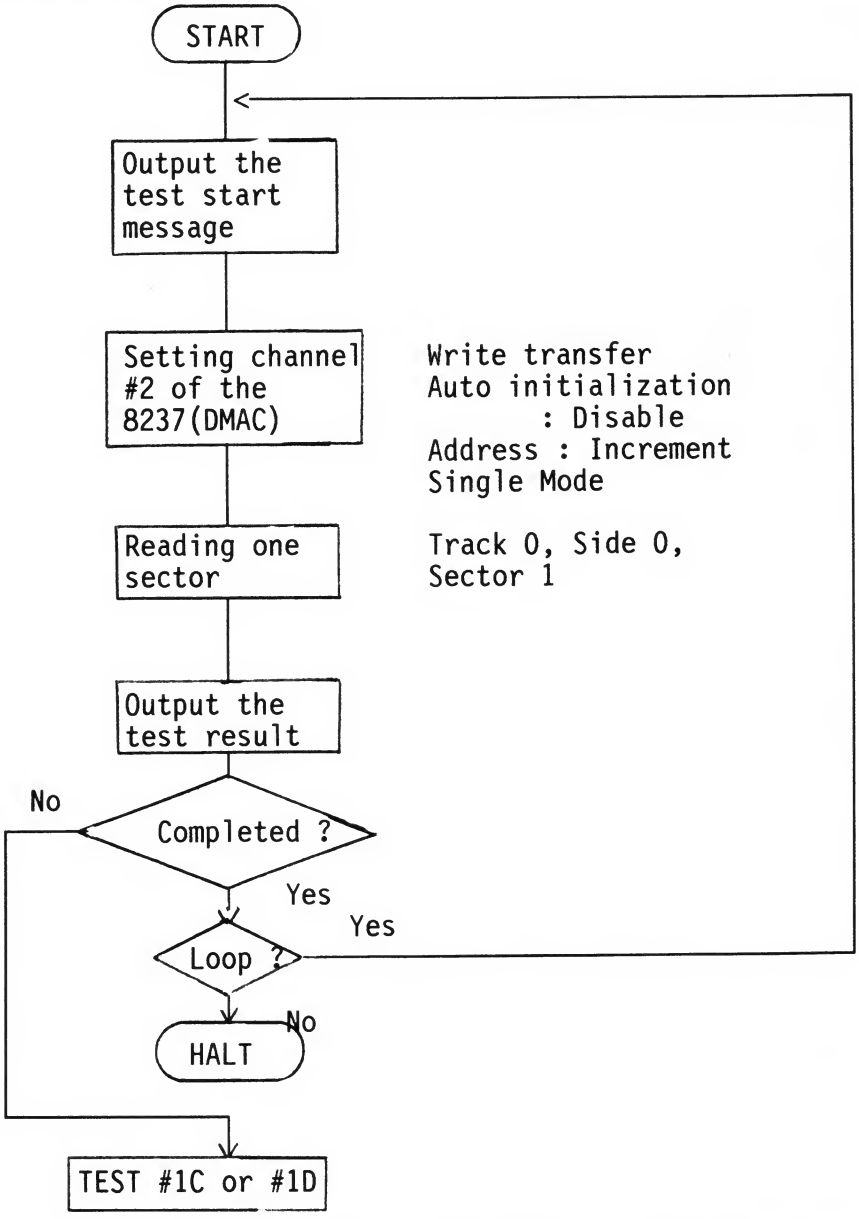
(REFER TO)

It is possible to check the FDD status signals - Step, Dir and Trk0 - during the loop mode (print out disable).

WAVEFORM - 23 .... WD37C65 Pin 28,38

TEST ITEM # 1B	TEST : FDD READ TEST

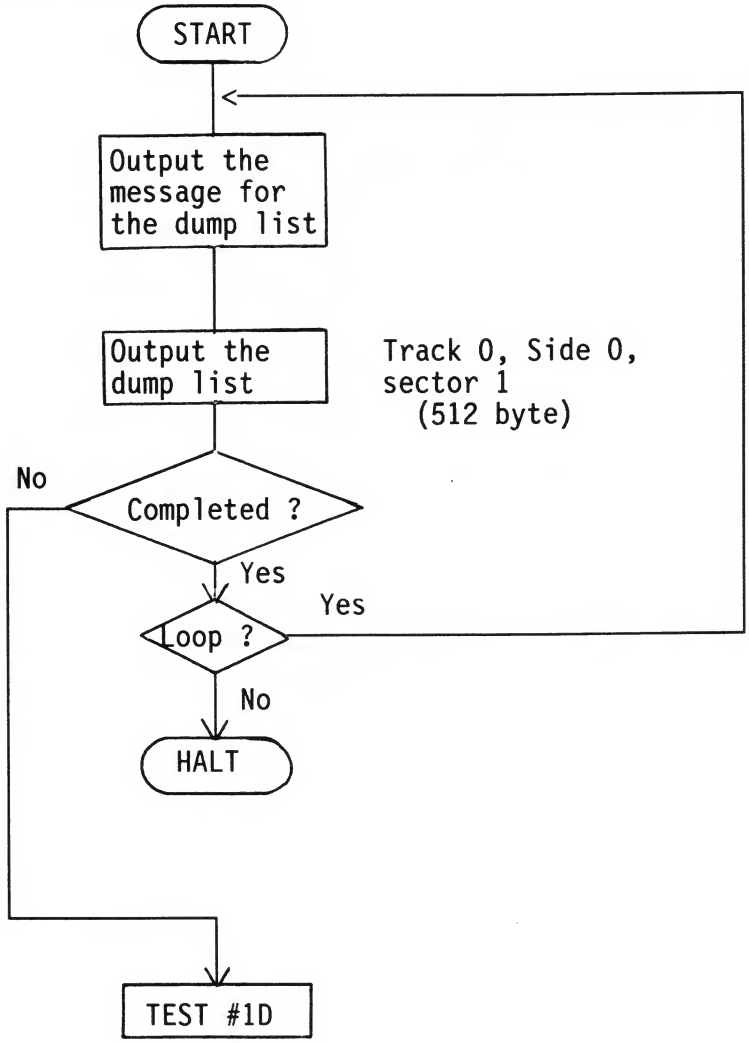
(DESCRIPTION)



(REFER TO)

TEST ITEM # 1C	TEST : OUTPUT OF THE DUMP LIST

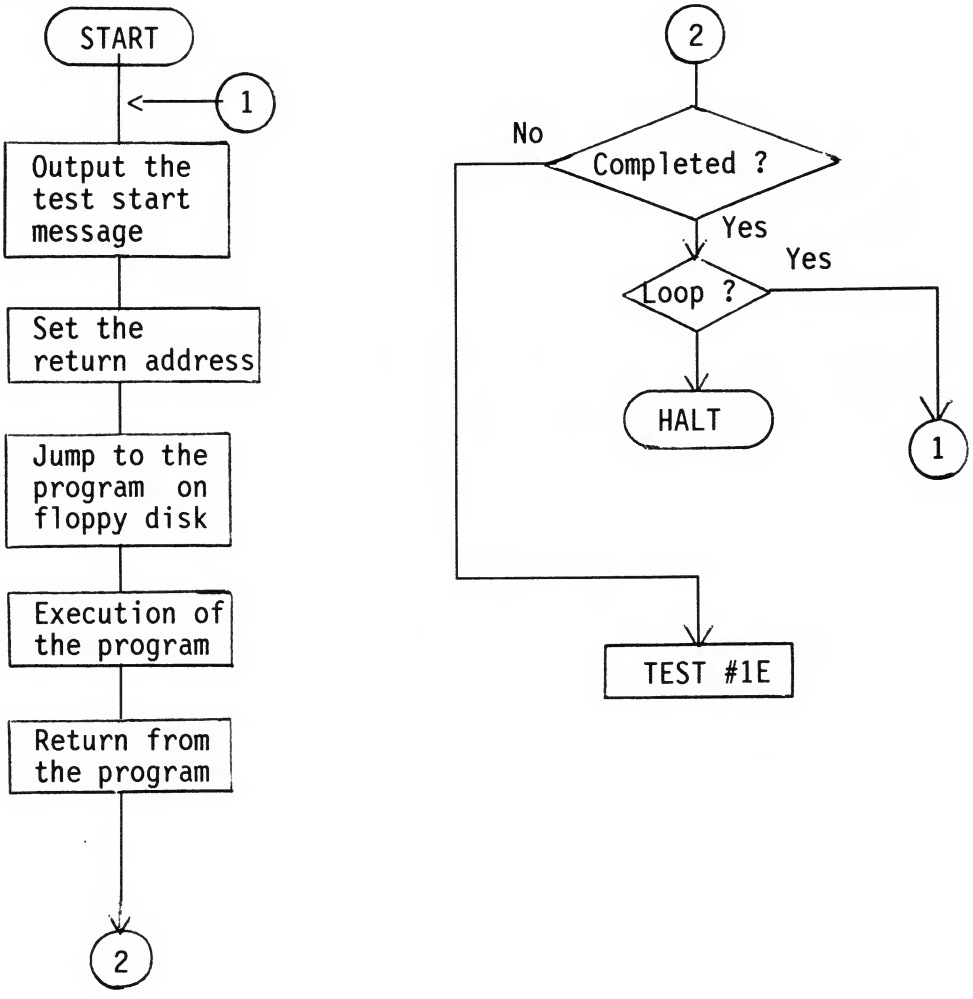
(DESCRIPTION)



(REFER TO)

TEST ITEM # 1D	TEST : JUMP TO THE PROGRAM LOADED FROM DISKETTE

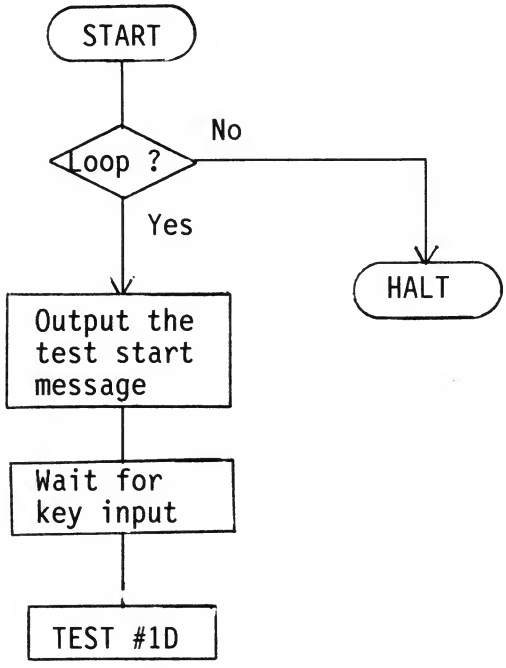
(DESCRIPTION)



(REFER TO)

TEST ITEM # 1F	TEST : EXCHANGE OF THE FLOPPY DISK

(DESCRIPTION)



(REFER TO)

EXAMPLE : TEST RESULT MESSAGE ON PRINTER

TEST RESULT IF NO ERROR DETECTED

```
ANDROMEDA Main Board Test Program

Test  4 .. ROM check sum ..................................................OK
Test  5 .. 8254 (in T4758(1B)) counter #1,#2,#3 1kHz
Test  6 .. Beep test
Test  7 .. 8254 (in T4758(1B)) counter #1 & Port B refresh detect .....OK
Test  8 .. DMAC (in T4758(1B)) register check .............................OK
Test  9 .. DMAC page register check .......................................OK
---- Set up DMAC !
Test  A .. 8042 - Key board interface test ................................OK
Test  B .. DRAM test (first 512k byte) ....................................OK
---- Setup stack now
Test  F .. Real Time Clock 146818(2D) battery backup check ................OK
Test 13 .. C-MOS RAM (in RTC 146818(2D)) Read/Write test ..................OK
Test 14 .. 8254 (in T4758(1B)) counter #0 .................................OK
Test 15 .. Setup interrupt controller
Test 16 .. Interrupt test (INT0) ..........................................OK
Test 17 .. Key board test .................................................OK
Test 18 .. Drive A: motor on
Test 19 .. Release FDC reset ...............................................OK
           FDD recalibrate test ..............................................OK
Test 1A .. Seek test .....................................................OK
Test 1B .. Read test and program loading ..................................OK

Test 1C .. Dump list (track : 00, side : 0, sector : 1, 512 byte)

0000: EA 08 00 FF FF EA F8 7F  00 F8 90 90 90 90 90 90    ................
0010: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0020: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0030: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0040: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0050: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0060: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0070: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0080: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0090: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00A0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00B0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00C0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00D0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00E0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
00F0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0100: 41 4E 44 52 4F 4D 45 44  41 20 74 65 73 74 20 44    ANDROMEDA test D
0110: 69 73 6B 65 74 74 65 90  90 90 90 90 90 90 90 90    iskette.........
0120: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0130: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0140: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0150: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0160: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0170: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0180: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
0190: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01A0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01B0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01C0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01D0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01E0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................
01F0: 90 90 90 90 90 90 90 90  90 90 90 90 90 90 90 90    ................

Test 1D .. reboot test
    Jump to boot program

    Return From Floppy Disk Based Test Program
```

TEST RESULT IF ERROR IS DETECTED

These test results mean that the ROM DIAGNOSTICS PROGRAM detects one or more error in the ANDROMEDA computer system.

***NOTE : In this case, the system has detected trouble on the RAS1 signal line (RAS1 selects the raw address of the last 128KB of RAM). This error can be detected by only TEST #C or #D.**

```
ANDROMEDA Main Board Test Program

Test  4 .. ROM check sum ..............................................OK
Test  5 .. 8254 (in T4758(1B)) counter #1,#2,#3 1kHz
Test  6 .. Beep test
Test  7 .. 8254 (in T4758(1B)) counter #1 & Port B refresh detect .....OK
Test  8 .. DMAC (in T4758(1B)) register check .........................OK
Test  9 .. DMAC page register check ...................................OK
---- Set up DMAC !
Test  A .. 8042 - Key board interface test ............................OK
Test  B .. DRAM test (first 512k byte) ................................OK
```

Produced by TEST #0B

```
ANDROMEDA Main Board Test Program

Test  4 .. ROM check sum ..............................................OK
Test  5 .. 8254 (in T4758(1B)) counter #1,#2,#3 1kHz
Test  6 .. Beep test
Test  7 .. 8254 (in T4758(1B)) counter #1 & Port B refresh detect .....OK
Test  8 .. DMAC (in T4758(1B)) register check .........................OK
Test  9 .. DMAC page register check ...................................OK
---- Set up DMAC !
Test  A .. 8042 - Key board interface test ............................OK
Test  C .. DRAM test (last 128k byte) .................................NG
    Parity error 4164 (1B,1C) bad!
    81464 (1A) bad!
    81464 (2A) bad!
    81464 (3A) bad!
    81464 (4A) bad!
```

Produced by TEST #0C

```
ANDROMEDA Main Board Test Program

Test  4 .. ROM check sum ..............................................OK
Test  5 .. 8254 (in T4758(1B)) counter #1,#2,#3 1kHz
Test  6 .. Beep test
Test  7 .. 8254 (in T4758(1B)) counter #1 & Port B refresh detect .....OK
Test  8 .. DMAC (in T4758(1B)) register check .........................OK
Test  9 .. DMAC page register check ...................................OK
---- Set up DMAC !
Test  A .. 8042 - Key board interface test ............................OK
Test  D .. DRAM test (640k byte) ......................................NG
```

Produced by TEST #0D

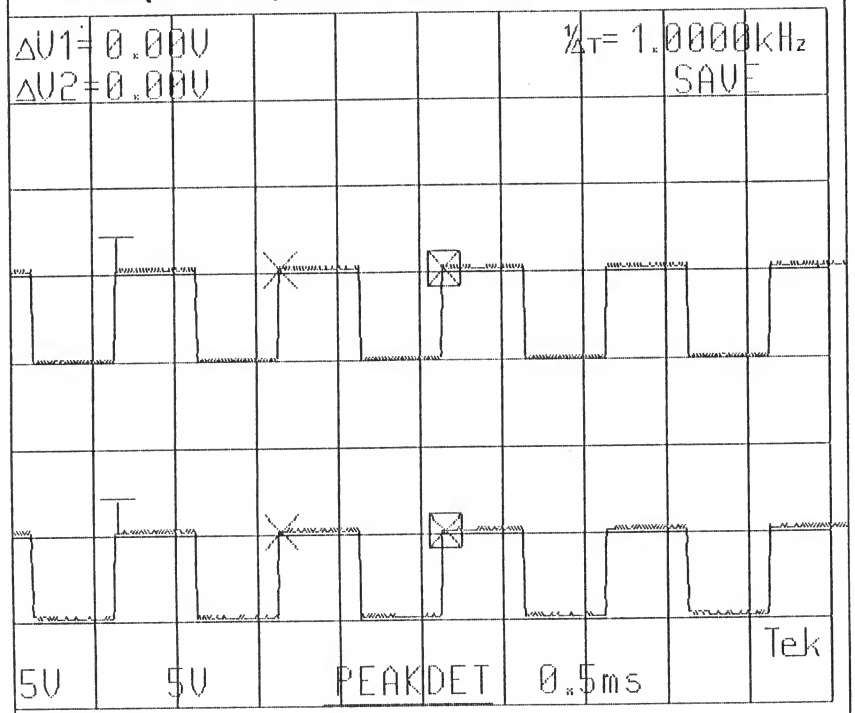
```
ANDROMEDA Main Board Test Program

Test  4 .. ROM check sum ..............................................OK
Test  5 .. 8254 (in T4758(1B)) counter #1,#2,#3 1kHz
Test  6 .. Beep test
Test  7 .. 8254 (in T4758(1B)) counter #1 & Port B refresh detect .....OK
Test  8 .. DMAC (in T4758(1B)) register check .........................OK
Test  9 .. DMAC page register check ...................................OK
---- Set up DMAC !
Test  A .. 8042 - Key board interface test ............................OK
Test  B .. DRAM test (first 512k byte) ................................OK
---- Setup stack now
Test  F .. Real Time Clock 146818(2D) battery backup check ............OK
Test 13 .. C-MOS RAM (in RTC 146818(2D)) Read/Write test ..............OK
Test 14 .. 8254 (in T4758(1B)) counter #0 .............................OK
Test 15 .. Setup interrupt controller
Test 16 .. Interrupt test (INT0) ......................................OK
Test 17 .. Key board test .............................................OK
Test 18 .. Drive A: motor on
Test 19 .. Release FDC reset ..........................................OK
           FDD recalibrate test .......................................OK
Test 1A .. Seek test ..................................................OK
Test 1B .. Read test and program loading ..............................OK
Test 1D .. reboot test
    Jump to boot program

    Return From Floppy Disk Based Test Program
```

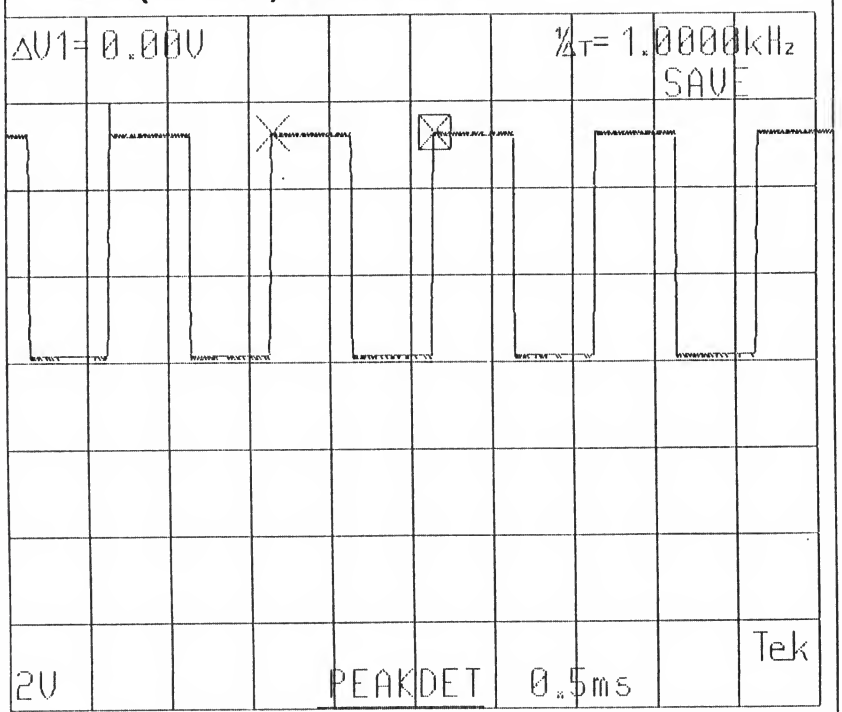
Produced by TEST #1D

WAVEFORM – 1 (TEST #5)
8254(in T4758) COUNTER #0,#1



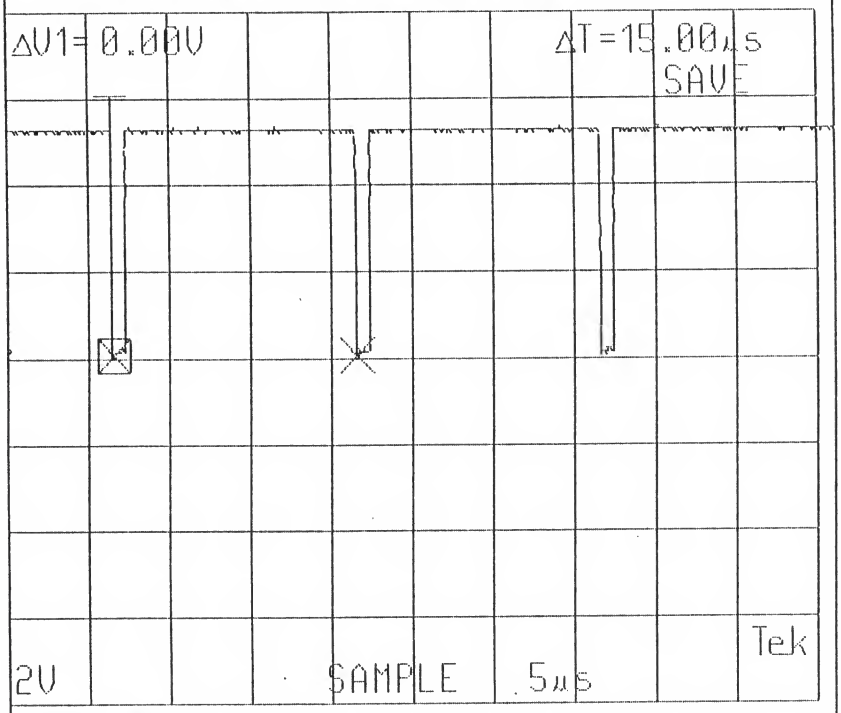
(TEST POINT)
CH1 : OUT0 (T4758(1B on ANDRO) pin 22)
CH2 : OUT1 (T4758(1B on ANDRO) pin 23)

WAVEFORM – 2 (TEST #5)
8254(in T4758) COUNTER #2



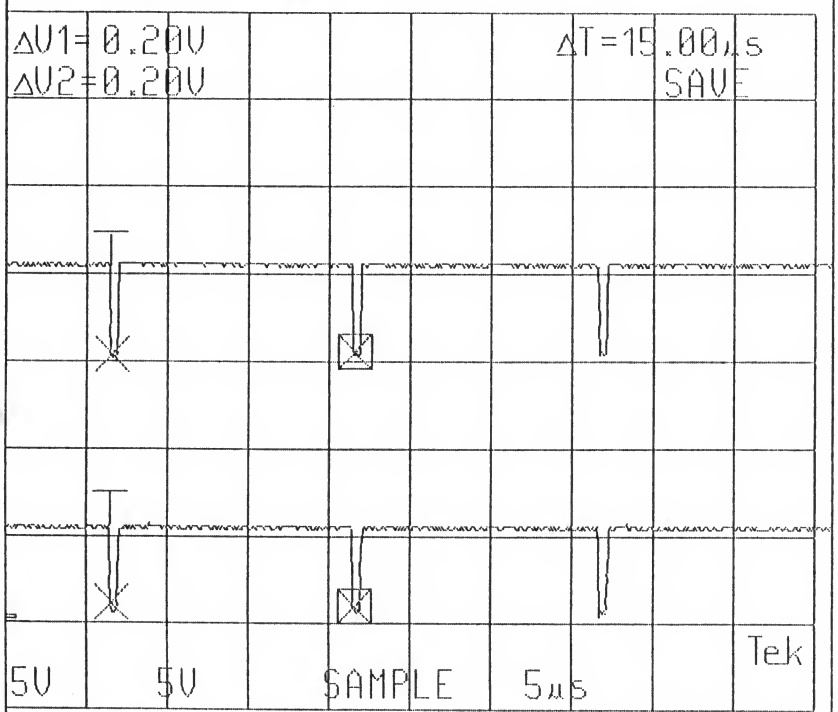
(TEST POINT) OUT2 (T4758(1B on ANDRO) pin 24)

WAVEFORM – 3 (TEST #7)
COUNTER #1 for DRAM REFRESH



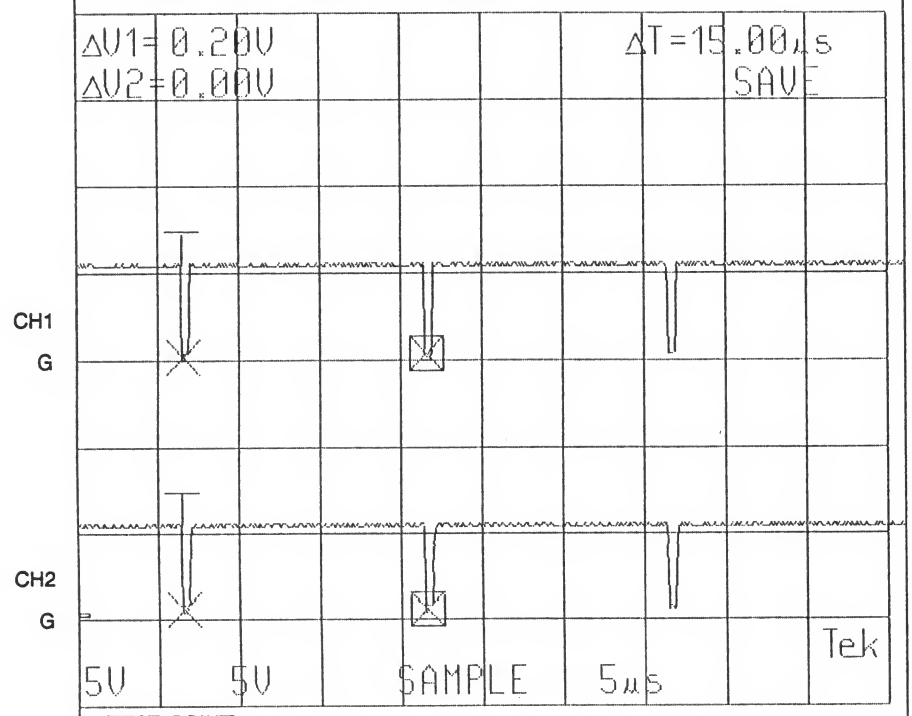
(TEST POINT)
OUT1 (T4758(1B on ANDRO) pin 23)

WAVEFORM – 4 (TEST #7)
REFRESH SIGNAL – (i)



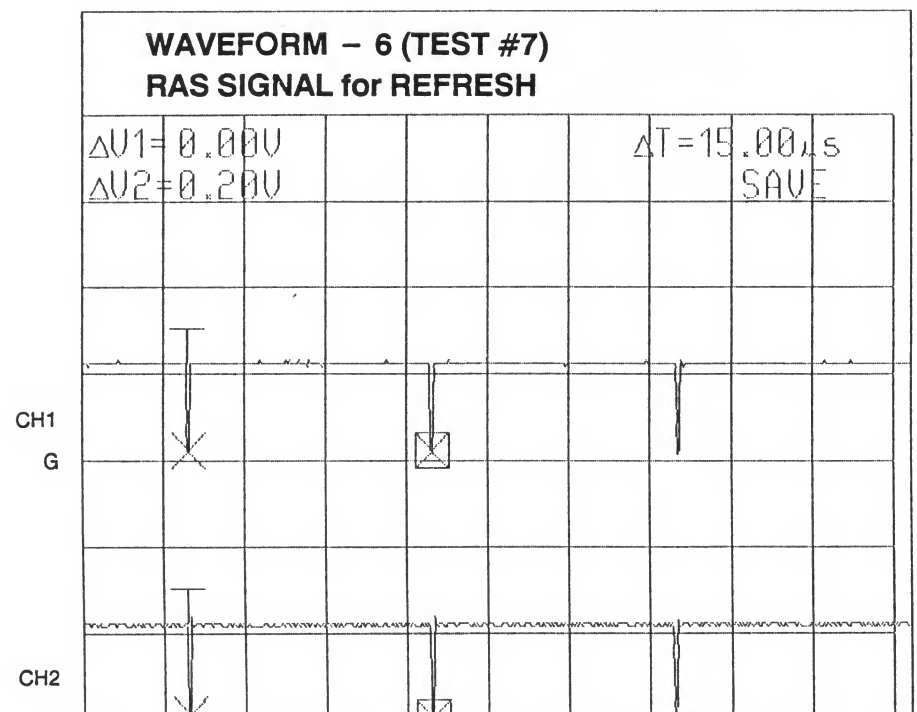
(TEST POINT)
CH1 : – RFO (GAATRF(6D on ANDRO) pin 28)
CH2 : – RFI (GAATRF(6D on ANDRO) pin 63)

WAVEFORM – 5 (TEST #7)
REFRESH SIGNAL – (ii)



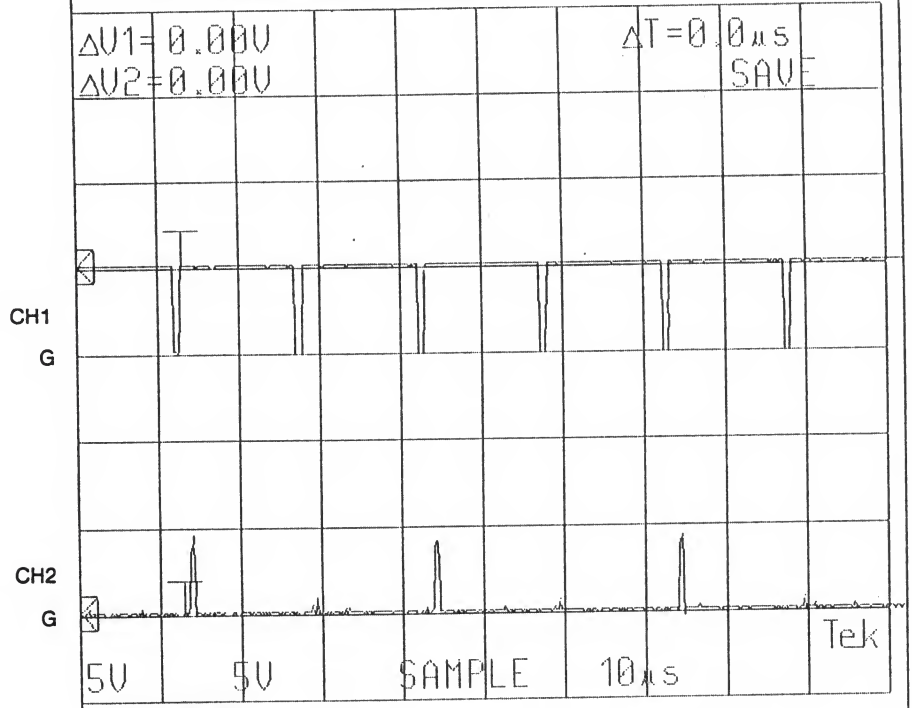
(TEST POINT)
CH1 : – RFO (GAATRF(6D on ANDRO) pin 28)
CH2 : – RFH (GAATIO(3C on ANDRO) pin 85)

WAVEFORM – 6 (TEST #7)
RAS SIGNAL for REFRESH



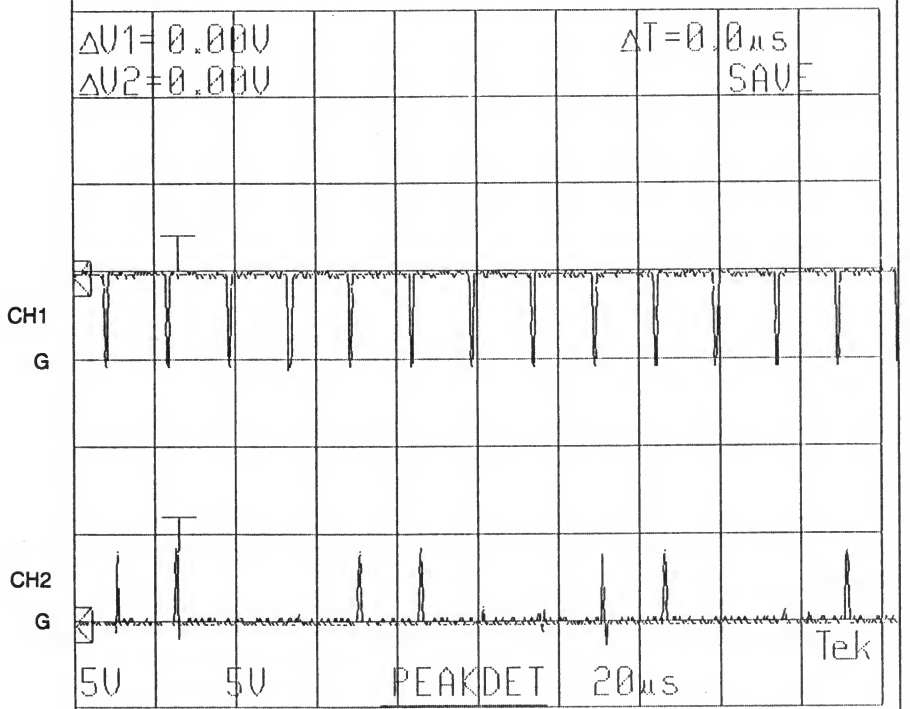
(TEST POINT)
CH1 : – RAS0 (GAATM2(8B on ADR – RM3) pin 60)
CH2 : – RAS1 (GAATM2(8B on ADR – RM3) pin 59)

WAVEFORM – 7 (TEST #7)
ADDRESS LINE 0 during REFRESH



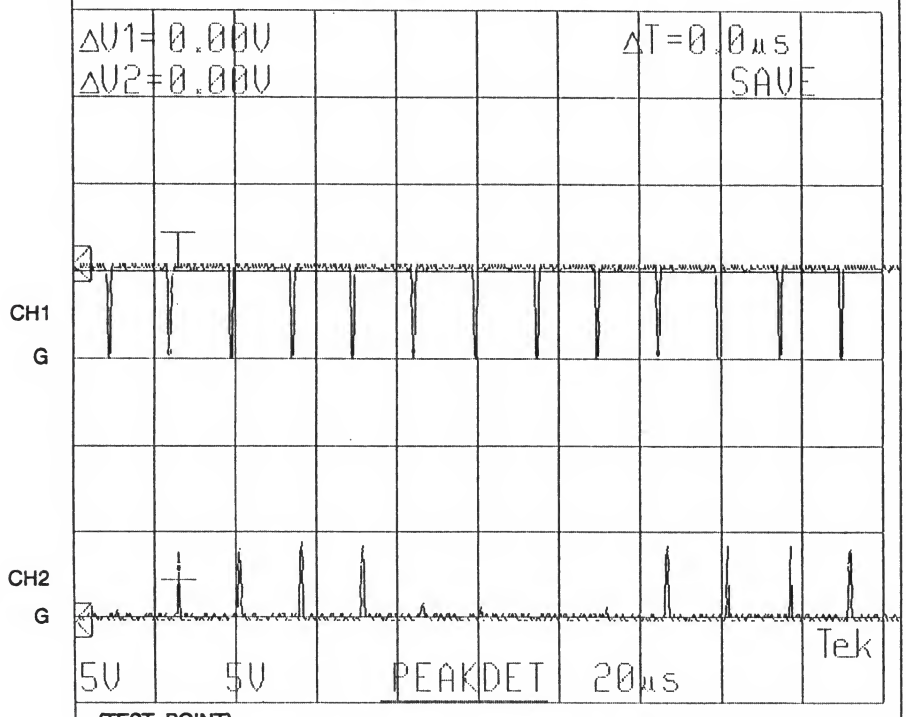
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA0 (GAATAB(6A on ANDRO) pin 11)

WAVEFORM – 8 (TEST #7)
ADDRESS LINE 1 during REFRESH



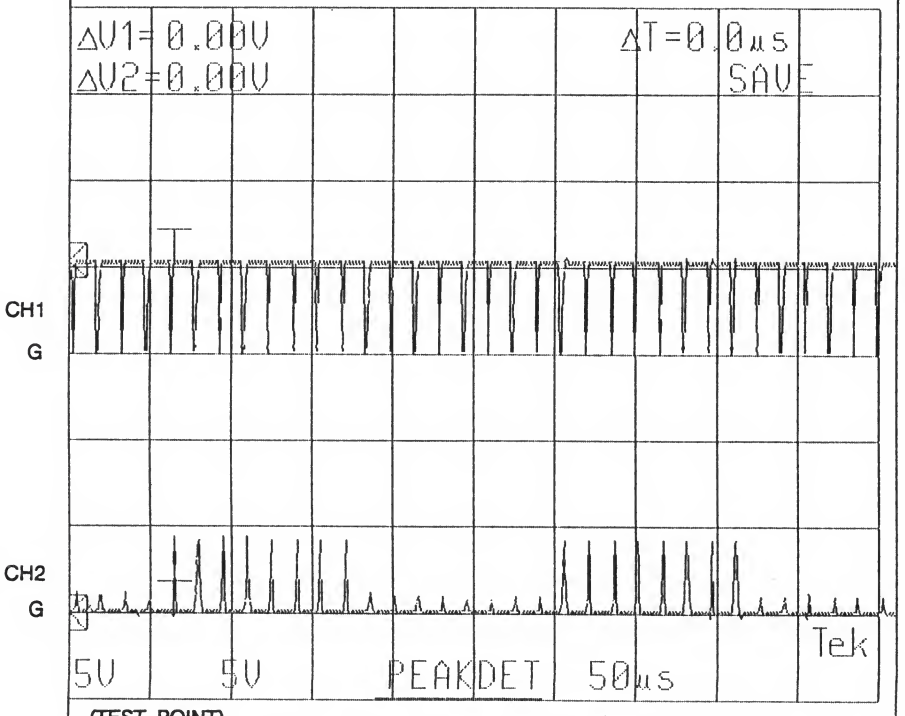
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA1 (GAATAB(6A on ANDRO) pin 12)

WAVEFORM – 9 (TEST #7)
ADDRESS LINE 2 during REFRESH



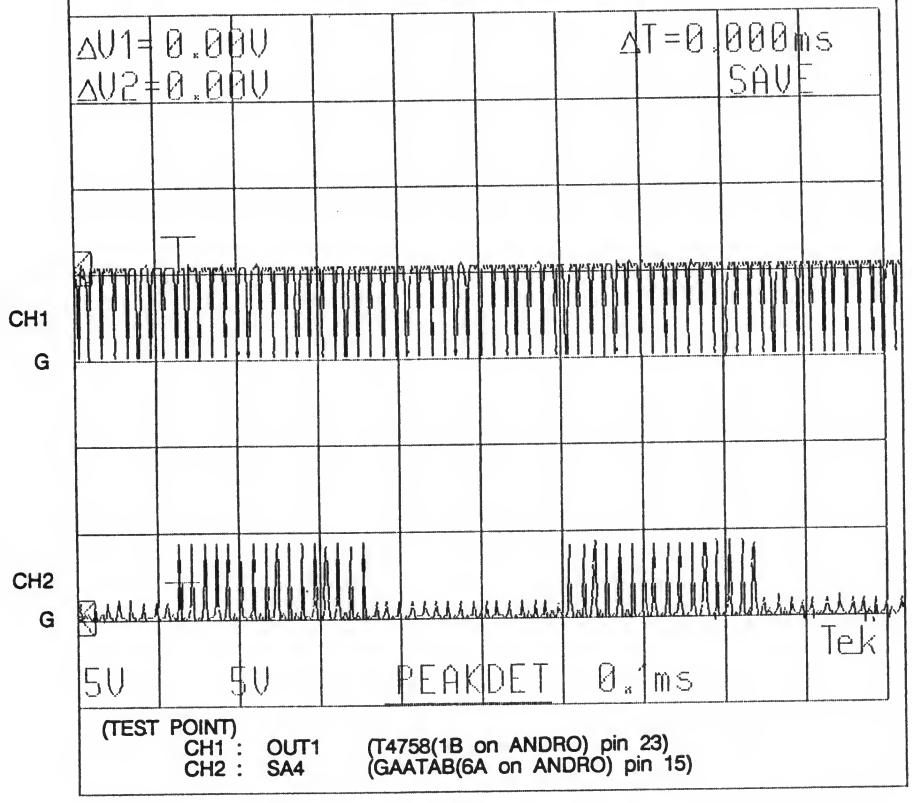
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA2 (GAATAB(6A on ANDRO) pin 13)

WAVEFORM – 10 (TEST #7)
ADDRESS LINE 3 during REFRESH



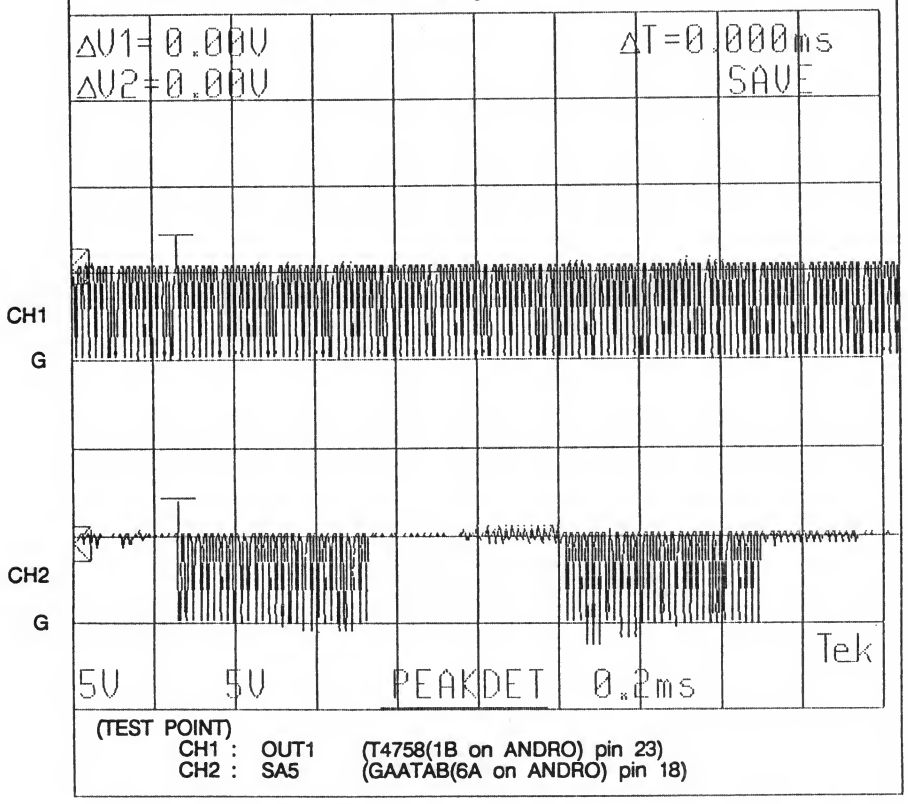
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA3 (GAATAB(6A on ANDRO) pin 14)

WAVEFORM – 11 (TEST #7)
ADDRESS LINE 4 during REFRESH



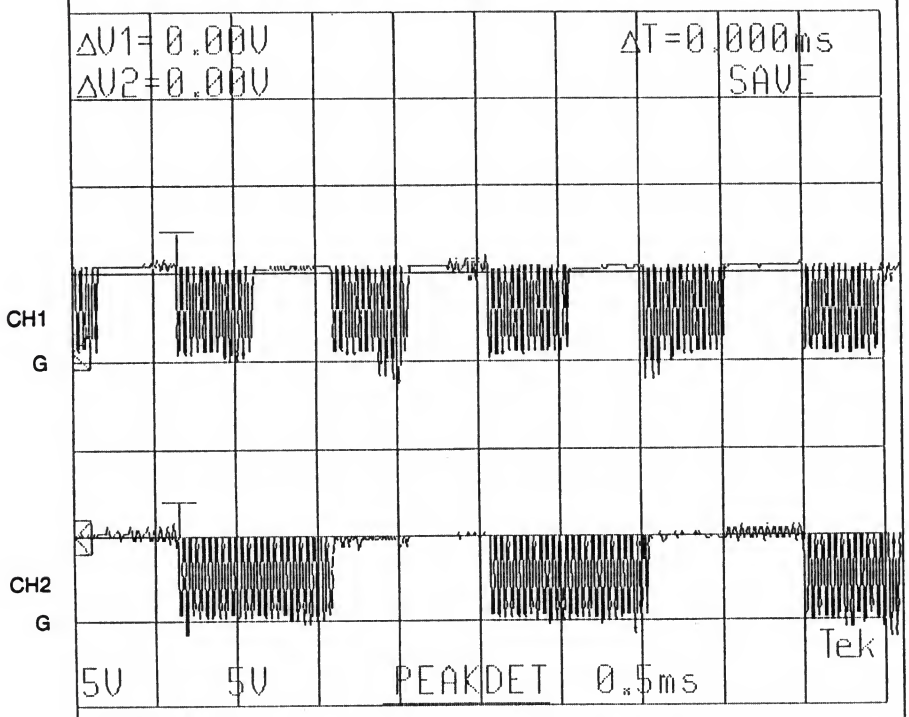
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA4 (GAATAB(6A on ANDRO) pin 15)

WAVEFORM – 12 (TEST #7)
ADDRESS LINE 5 during REFRESH



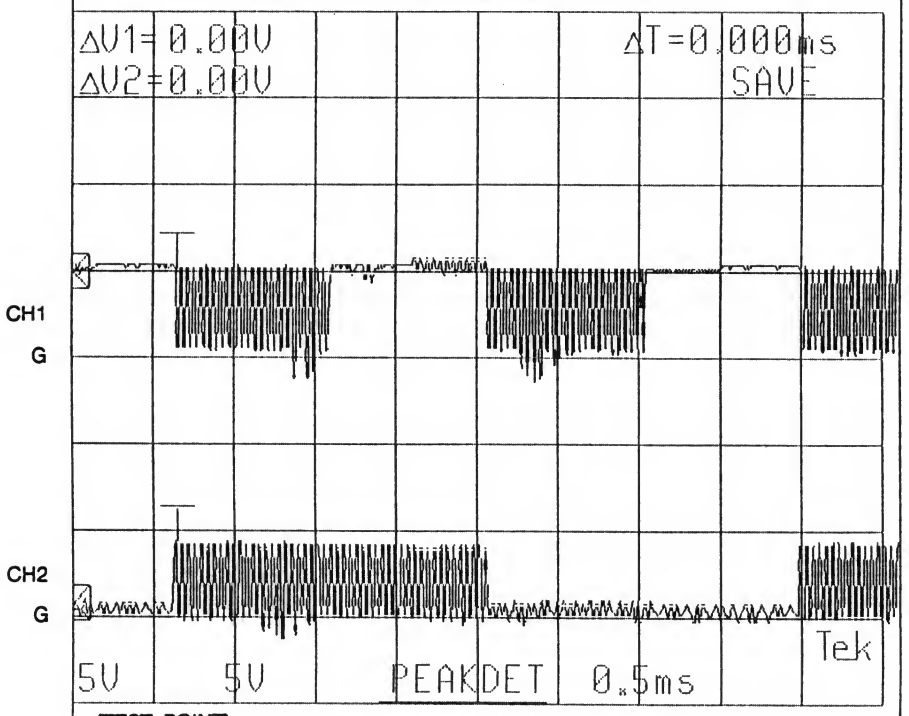
(TEST POINT)
CH1 : OUT1 (T4758(1B on ANDRO) pin 23)
CH2 : SA5 (GAATAB(6A on ANDRO) pin 18)

WAVEFORM – 13 (TEST #7)
ADDRESS LINE 6 during REFRESH



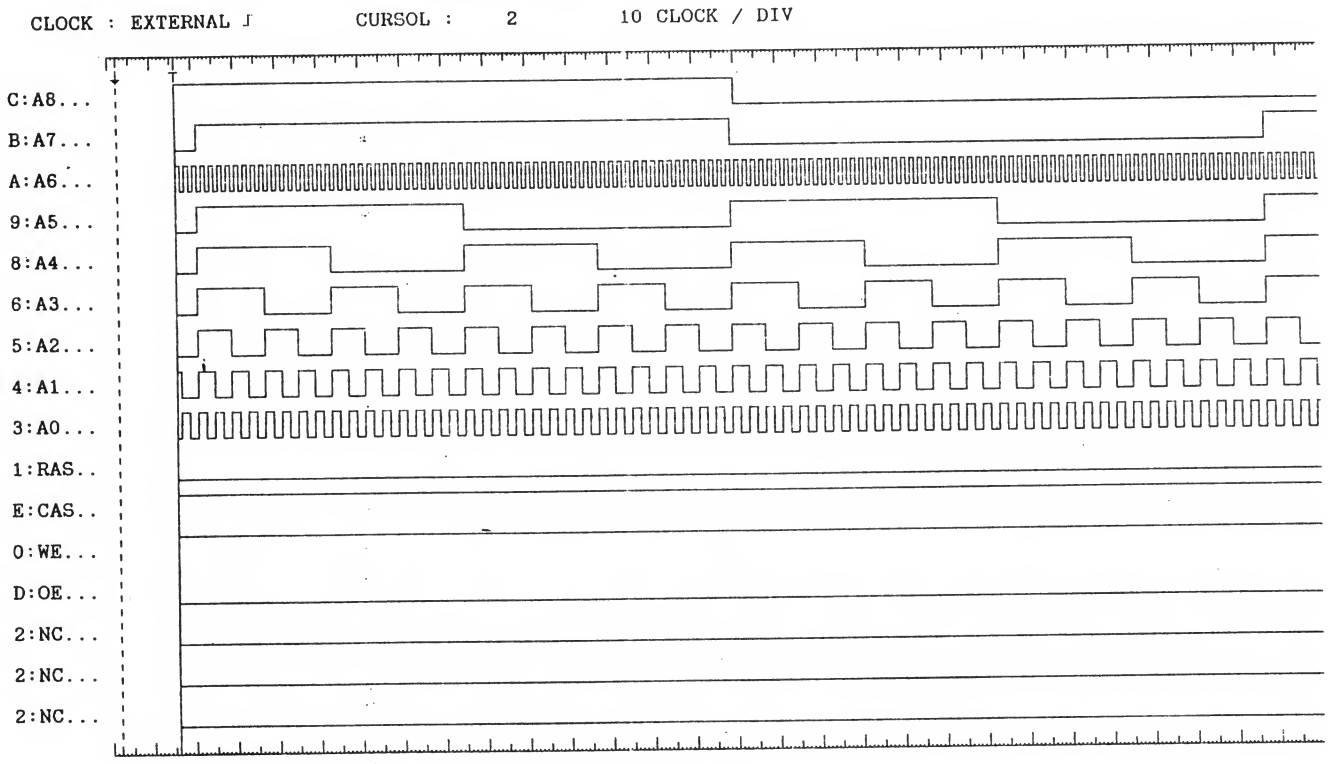
(TEST POINT)
CH1 : SA5 (GAATAB(6A on ANDRO) pin 18)
CH2 : SA6 (GAATAB(6A on ANDRO) pin 19)

WAVEFORM – 14 (TEST #7)
ADDRESS LINE 7 during REFRESH

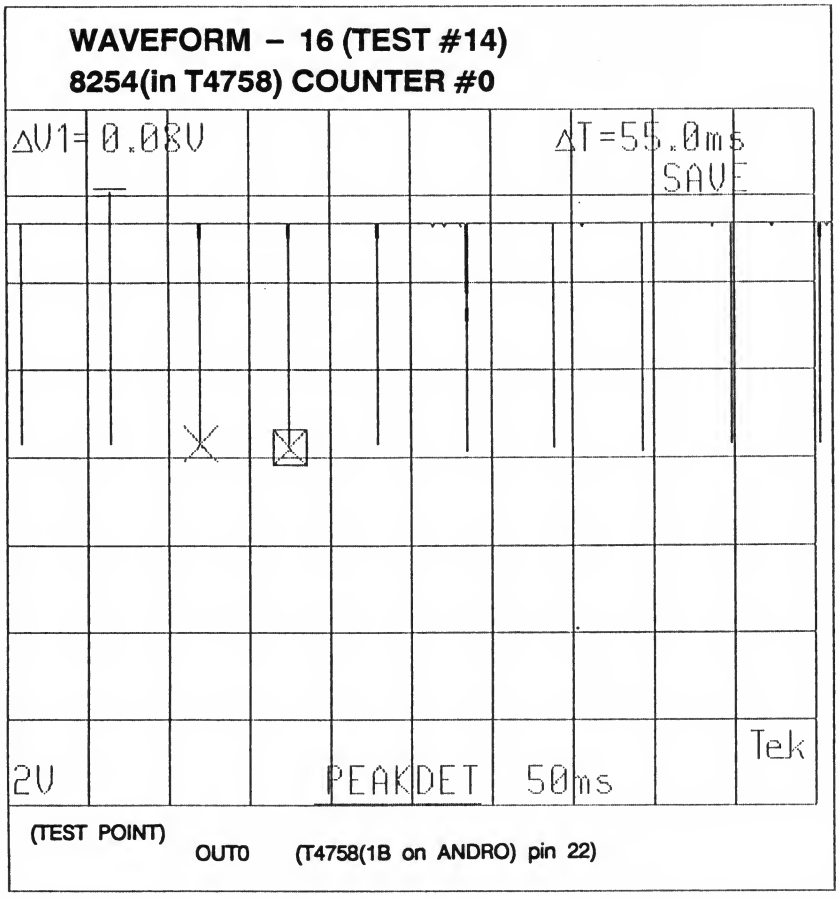


(TEST POINT)
CH1 : SA6 (GAATAB(6A on ANDRO) pin 19)
CH2 : SA7 (GAATAB(6A on ANDRO) pin 20)

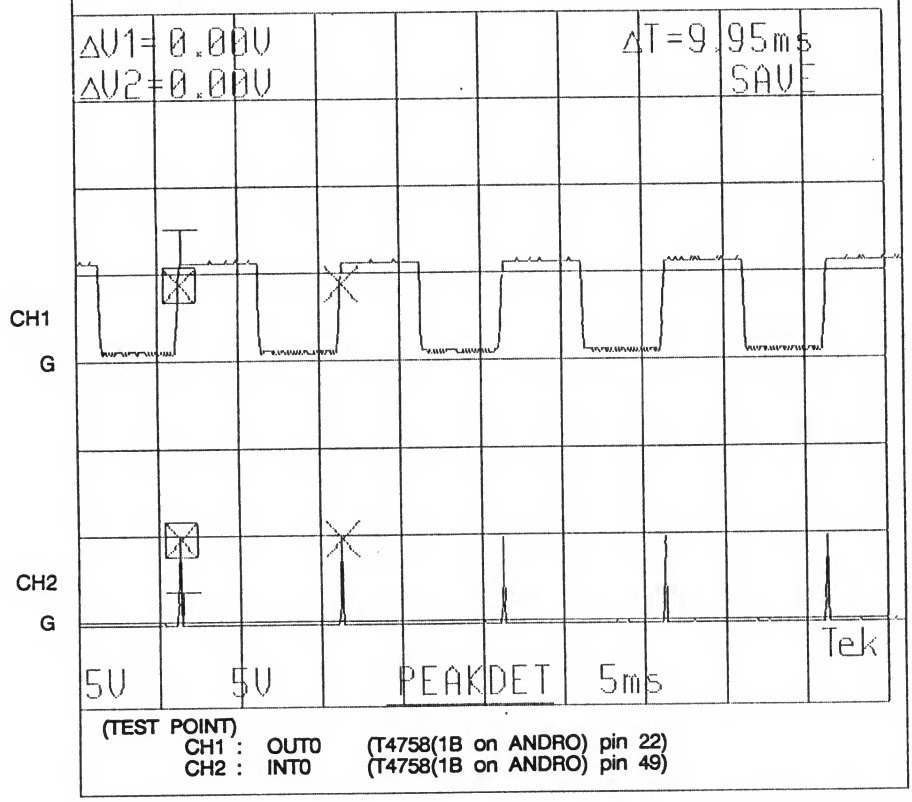
WAVEFORM – 15 (TEST #7)
ADDRESS BUS during REFRESH



WAVEFORM – 16 (TEST #14)
8254(in T4758) COUNTER #0

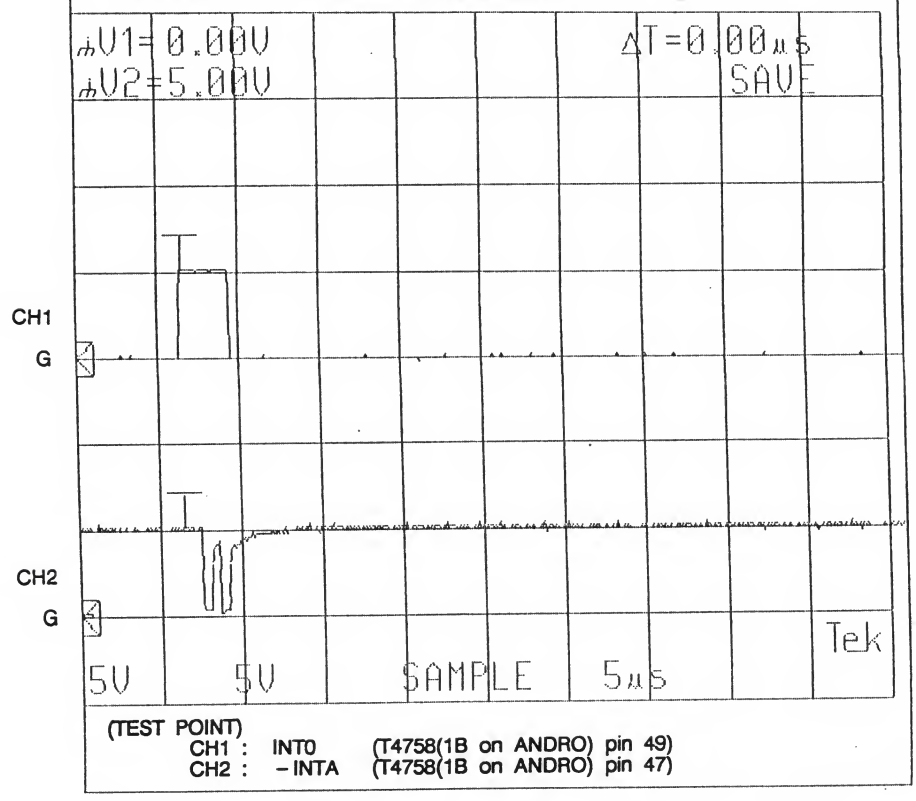


WAVEFORM – 17 (TEST #16)
INTERRUPT SIGNAL to CPU



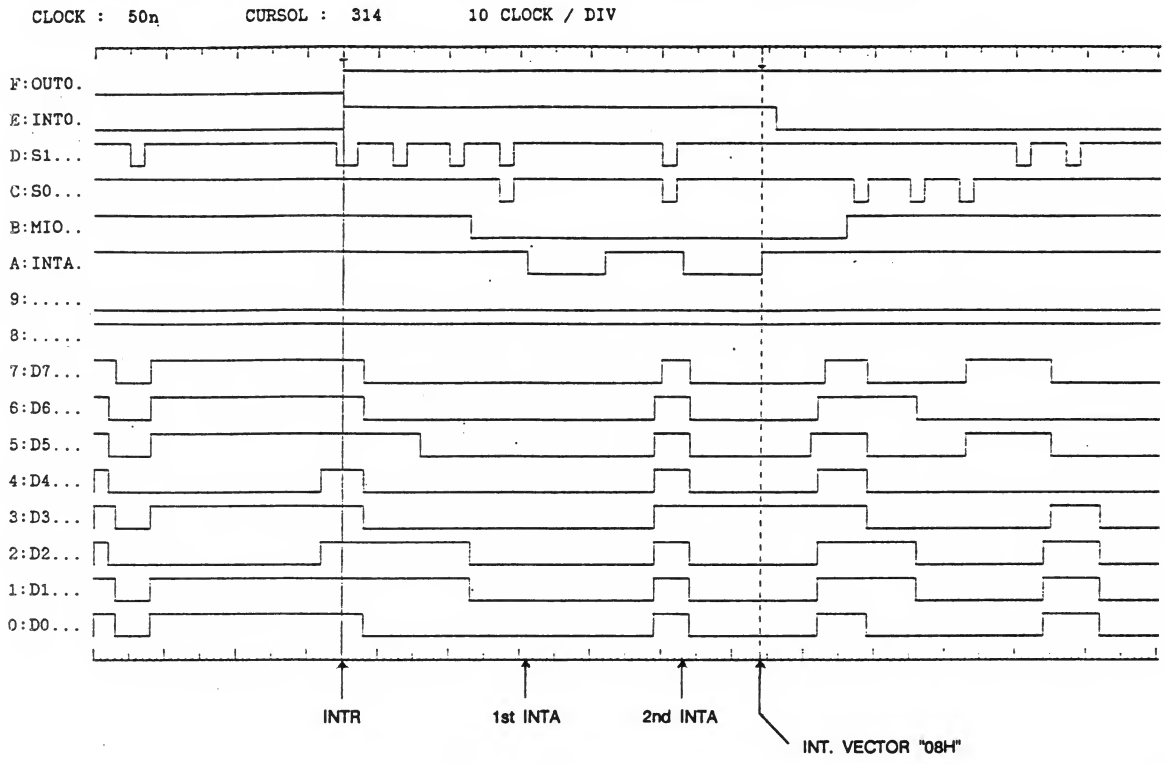
(TEST POINT)
CH1 : OUT0 (T4758(1B on ANDRO) pin 22)
CH2 : INT0 (T4758(1B on ANDRO) pin 49)

WAVEFORM – 18 (TEST #16)
INTERRUPT ACKNOWLEDGE

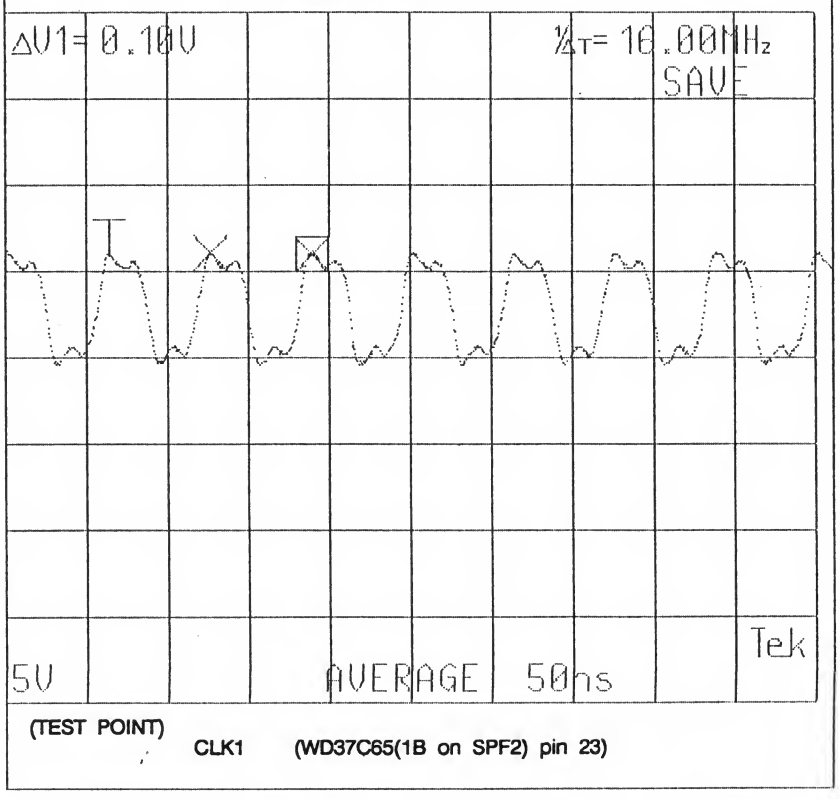


(TEST POINT)
CH1 : INT0 (T4758(1B on ANDRO) pin 49)
CH2 : –INTA (T4758(1B on ANDRO) pin 47)

WAVEFORM – 19 (TEST #16)
INTERRUPT SEQUENCE

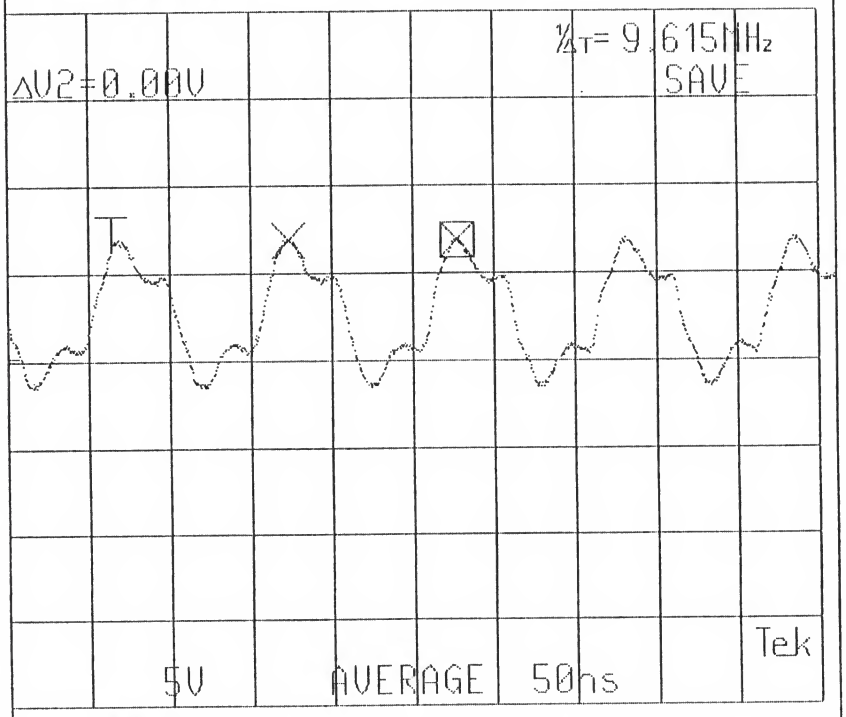


WAVEFORM – 20 (TEST #18)
CLOCK for FDSSC – (i)



G

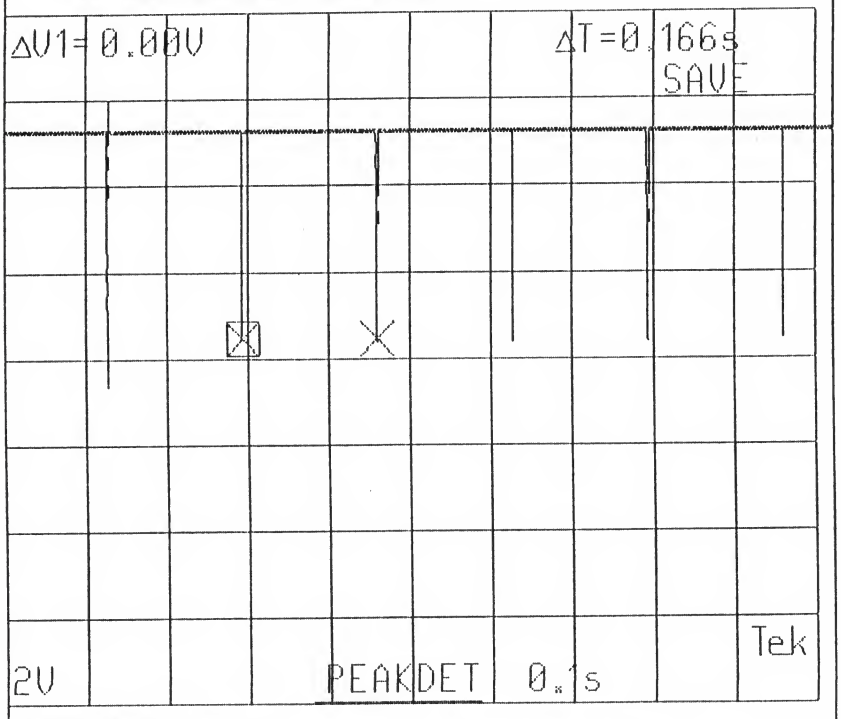
WAVEFORM – 21 (TEST #18)
CLOCK for FDSSC – (ii)



G

(TEST POINT) CLK2 (WD37C65(1B on SPF2) pin 21)

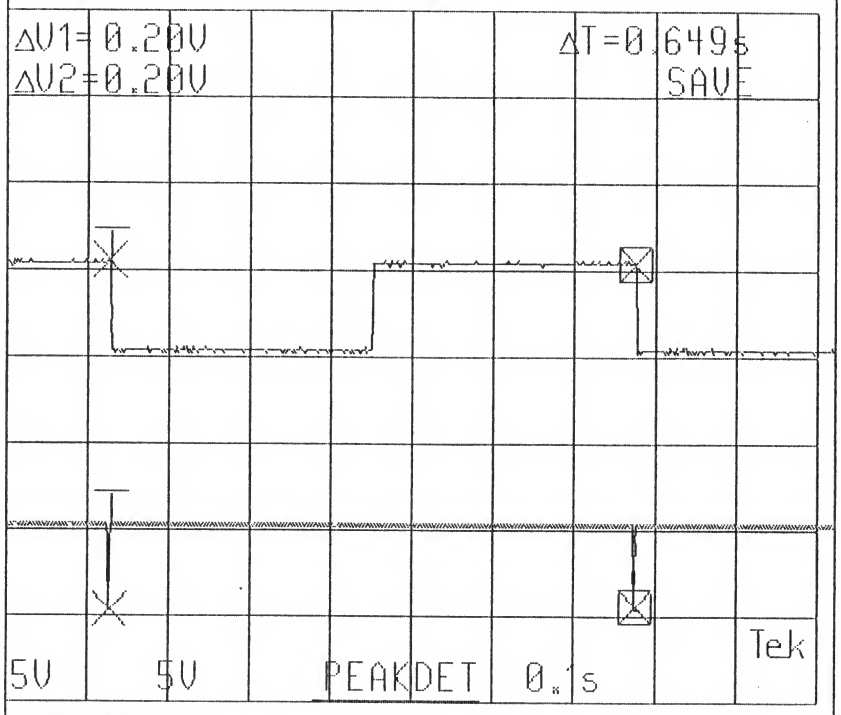
WAVEFORM – 22 (TEST #18)
INDEX SIGNAL from FDD



G

(TEST POINT) – IDX (WD37C65(1B on SPF2) pin 39)

WAVEFORM – 23 (TEST #1A)
DIRECTION & TRACK – 00



(TEST POINT)
CH1 : – DIRC (WD37C65(1B on SPF2) pin 28)
CH2 : – TR00 (WD37C65(1B on SPF2) pin 38)

CHAPTER 5

DISASSEMBLY AND ASSEMBLY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

5.1 GENERAL REPAIR INFORMATION

This section provides procedures for removal and replacement of the major subassemblies of EQUITY II+/EPSON PC AX2, and includes a list of tools with EPSON part numbers. These tools are also commercially available.

TABLE 5-1. REPAIR TOOLS AND EQUIPMENT

TOOLS	PART NUMBER
Phillips screwdriver (#1)	B743800100
Phillips screwdriver (#2)	B743800200

WARNING

The circuit boards contain static-sensitive CMOS IC and must be handled with care. Discharge bodily static before removing circuit boards, and wear a grounded wrist strap during disassembly. Place the boards on rubber mats or similar non-static surfaces when they are removed from the case.

5.2 MAIN UNIT DISASSEMBLY AND ASSEMBLY

The following pages describe and illustrate the procedures to be used for the removal and the replacement of components of the main unit.

5.2.1 COVER REMOVAL

Refer to the illustration shown in Figure 5 – 1.

1. Remove the five screws (labeled A).
2. Slide the cover (labeled B) away from you for 10cm.
3. Lift the cover away from the computer.

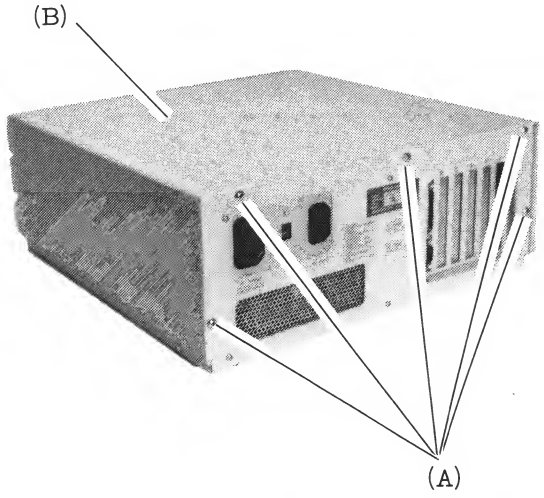


FIGURE 5 – 1. COVER REMOVAL/REPLACEMENT

5.2.2 COVER REPLACEMENT

Refer to Figure 5 – 1, above.

1. Hold the cover (B), and lower it onto the computer, then slide the cover back until the back panal is just inside the edge of the cover.
2. Replace the five screws (A) that secure the cover to the chassis.

5.2.3 FRONT PANEL REMOVAL

Refer to Figure 5 – 2, which illustrates this procedure.

1. Remove the cover. (Refer to Section 5.2.1.)

2. Remove the five screws (labeled A) to remove the front panel (labeled B).

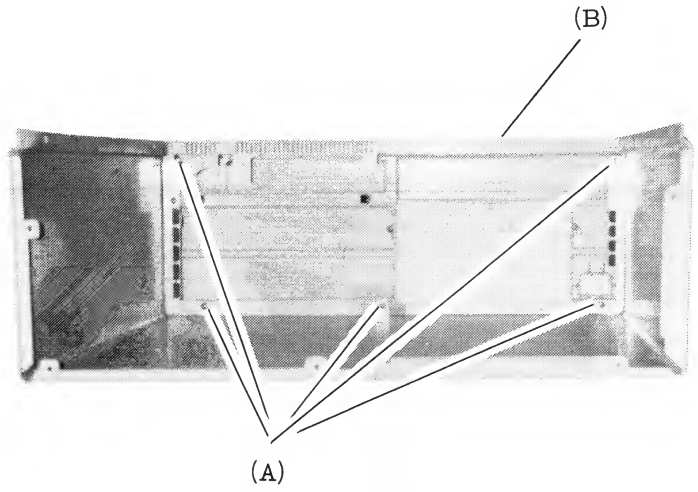


FIGURE 5 – 2. FRONT PANEL REMOVAL/REPLACEMENT

5.2.4 FRONT PANEL REPLACEMENT

Refer to Figure 5 – 2, above.

1. Replace the front panel by attaching the five screws (A) and plates (labeled B).

2. Replace the cover. (Refer to Section 5.2.2).

5.2.5 POWER SUPPLY (ADRPS) UNIT REMOVAL

Figure 5 – 3 illustrates the procedure described in this section.

1. Remove the cover. (Refer to Section 5.2.1).
2. Remove the two ANDRO Board connectors (labeled A) and the FDD and HDD power supply connectors.
3. Pull out the power switch extension stick (labeled B) from the power supply unit.
4. Remove the four screws (labeled C) from the rear.
5. Slide the power supply unit (labeled D) about 2 cm toward the front to clear the hold – down tabs and remove the unit.

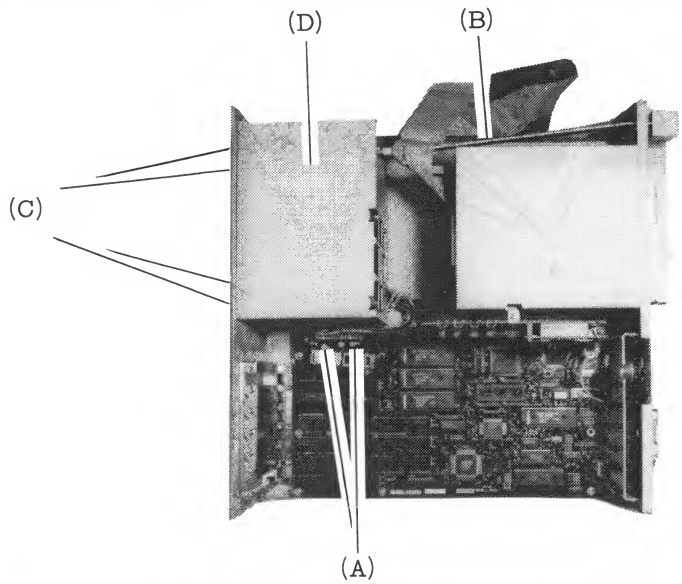


FIGURE 5 – 3. POWER SUPPLY (ADRPS) UNIT REMOVAL/REPLACEMENT

5.2.6 POWER SUPPLY (ADRPS) UNIT REPLACEMENT

Refer to the Figure 5 – 3, above.

1. Replace the power supply unit by sliding it toward the rear over the hold – down tabs on the lower case.
2. Fasten the power supply unit with the four screws (C).
3. Insert the power switch extension stick (B) into the power switch of the power supply unit.
4. Connect the two connectors (A) and the FDD and HDD connectors.
5. Replace the cover. (Refer to Section 5.2.2).

5.2.7 OPTION CARD REMOVAL

The illustration for this procedure is Figure 5 – 4, below.

1. Remove the cover. (Refer to Section 5.2.1).
2. Disconnect the cables attached to the option card, if required.
3. Remove one screw (labeled A) to release the option card.
4. Lift the option card straight up.

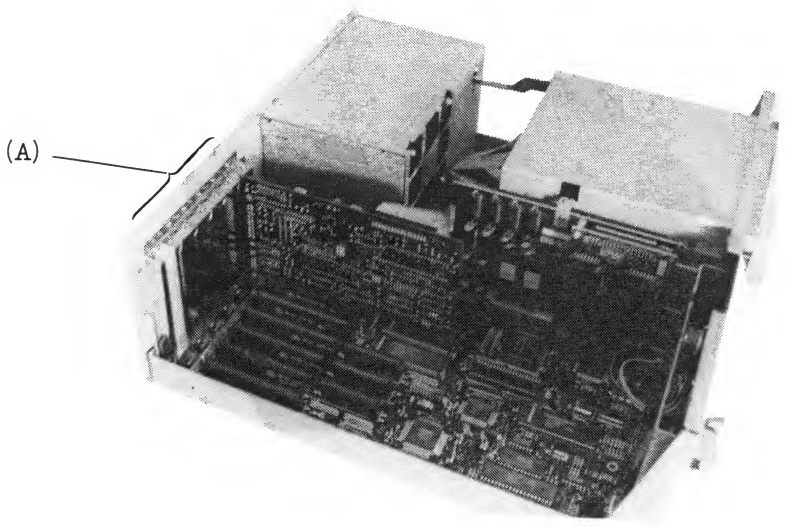


FIGURE 5 – 4. OPTION CARD REMOVAL/REPLACEMENT

5.2.8 OPTION CARD REPLACEMENT

Refer to Figure 5 – 4, above.

1. Install the option card in an appropriate option slot (16 – bit bus or 8 – bit bus).
2. Install one screw (A) to secure the option card.
4. Connect the cable connectors.
5. Replace the cover. (Refer to Section 5.2.2)

5.2.9 AUDIO SPEAKER REMOVAL

Refer to Figure 5 – 5 as the illustration for the instructions below.

1. Remove the cover. (Refer to Section 5.2.1)
2. Disconnect the connector (labeled A), and remove the screw (labeled B) from the audio speaker. If necessary, remove the system memory board (using the procedure given in Section 5.2.15).
3. Lift out the audio speaker.

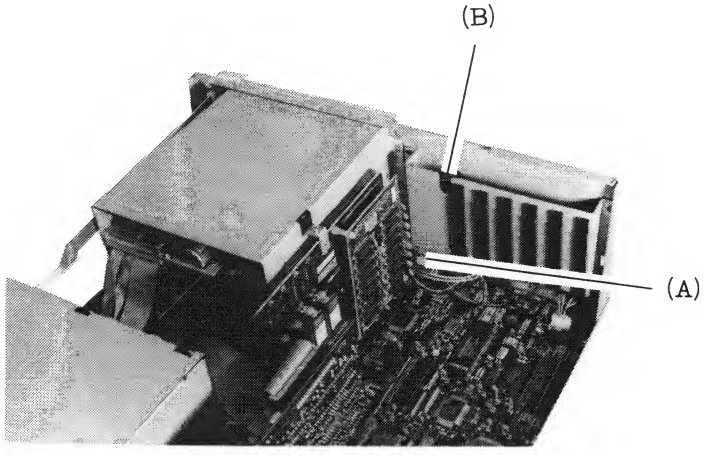


FIGURE 5 – 5. AUDIO SPEAKER REMOVAL/REPLACEMENT

5.2.10 AUDIO SPEAKER REPLACEMENT

Refer to Figure 5 – 5, above.

1. Replace the audio speaker.
2. Connect the connector (A), and secure the audio speaker with the screw (B).
3. Replace the cover. (Refer to Section 5.2.2.)

5.2.11 POWER – ON LED ASSEMBLY REMOVAL

See Figure 5 – 6 for an illustration of this procedure.

1. Remove the cover. (Refer to Section 5.2.1)
2. Disconnect two connectors to the power – on LED assembly (labeled A), and remove the screw (labeled B) from the power – on LED assembly. If necessary, remove the system memory board (using the procedure given in Section 5.2.15).

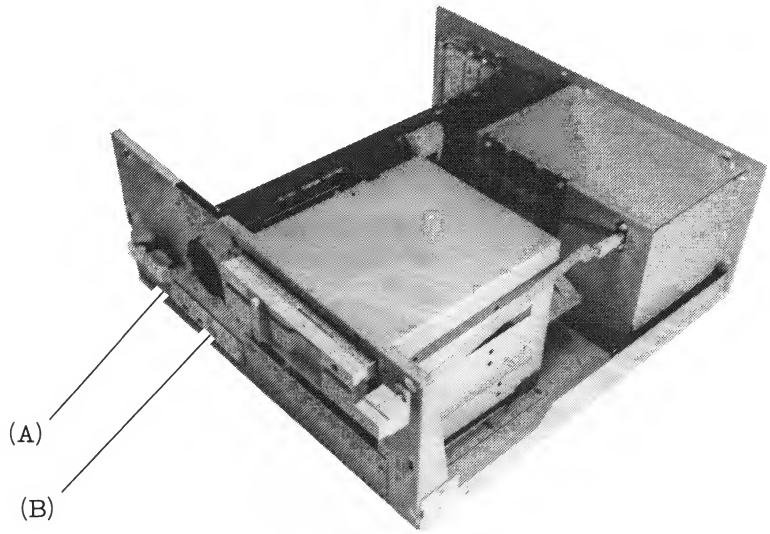


FIGURE 5 – 6. POWER – ON LED ASSEMBLY REMOVAL/REPLACEMENT

5.2.12 POWER – ON LED ASSEMBLY REPLACEMENT

Refer to Figure 5 – 6, above.

1. Replace the power – on LED assembly.
2. Connect two connectors to the power – on LED assembly (A).
3. Ensure that the power – on LED assembly tabs are fitted into the lower case holes, then secure the power – on LED assembly with the screw (B).
4. Replace the cover. (Refer to Section 5.2.2)

5.2.13 MAIN CONTROL BOARD (ANDRO BOARD) REMOVAL

Figure 5 – 7 below illustrates these instructions.

1. Remove the cover. (Refer to Section 5.2.1)
2. Remove the all option cards. (Refer to Section 5.2.7)
3. Remove the system memory board. (Refer to Section 5.2.15)
4. Disconnect the six connectors labeled A (two power cable connectors, one lithium battery connector, one audio speaker connector, one power – on LED connector, one keyboard connec – tor).
5. Remove seven screws (labeled B), then lift up the main control board unit.

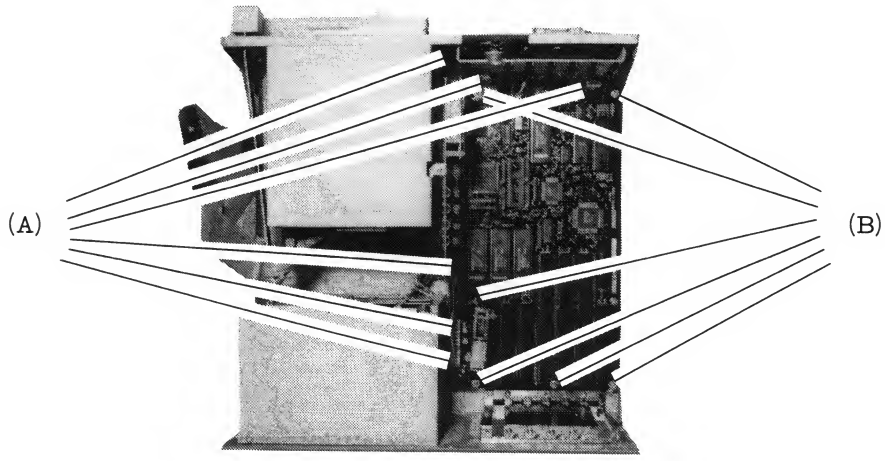


FIGURE 5 – 7. MAIN CONTROL BOARD (ANDRO BOARD) REMOVAL/REPLACEMENT

5.2.14 MAIN CONTROL BOARD (ANDRO BOARD) REPLACEMENT

Refer to Figure 5 – 7, above.

1. Replace the main control board in the lower case, and secure the board with seven screws (B).
2. Connect the six connectors (A).
3. Replace the system memory board. (Refer to Section 5.2.16)
4. Replace all option cards. (Refer to Section 5.2.8)
5. Replace the cover. (Refer to Section 5.2.2)

5.2.15 SYSTEM MEMORY BOARD (ADR – RM3/ADR – RM3S) REMOVAL

Refer to Figure 5 – 8 below illustrates these instructions.

1. Remove the cover. (Refer to Section 5.2.1)
2. Remove the one screw (labeled B), and lift out the system memory board (ADR – RM3/ADR – RM3S) labeled (B).

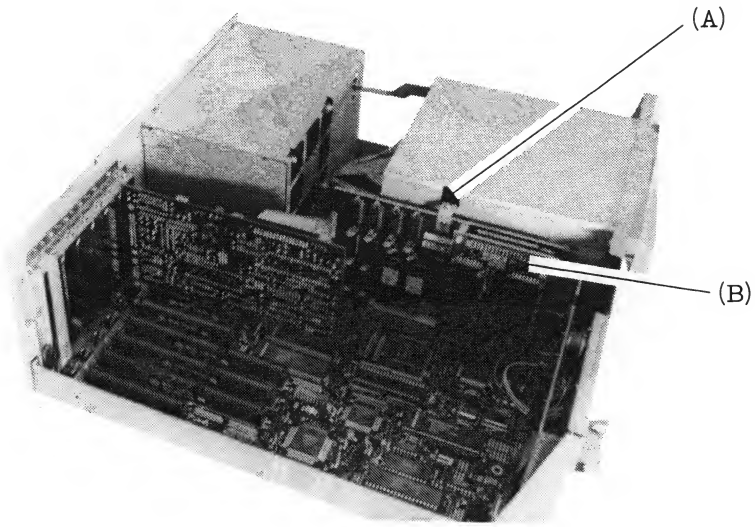


FIGURE 5 – 8. SYSTEM MEMORY BOARD REMOVAL/REPLACEMENT

5.2.16 SYSTEM MEMORY BOARD (ADR – RM3/ADR – RM3S) REPLACEMENT

Refer to Figure 5 – 8 above.

1. Replace the system memory board (B), then secure it with the single screw (A).
2. Replace the cover. (Refer to Section 5.2.2)

5.2.17 DISK DRIVE UNIT (FDD OR HDD) REMOVAL

Refer to Figure 5-9 below.

1. Remove the cover. (Refer to Section 5.2.1)
2. Disconnect the signal and power supply cables on the rear of the drive unit.
3. Remove the two screws (labeled A) fastening the drive.
4. Remove the drive unit by sliding it carefully out the front of the lower case.

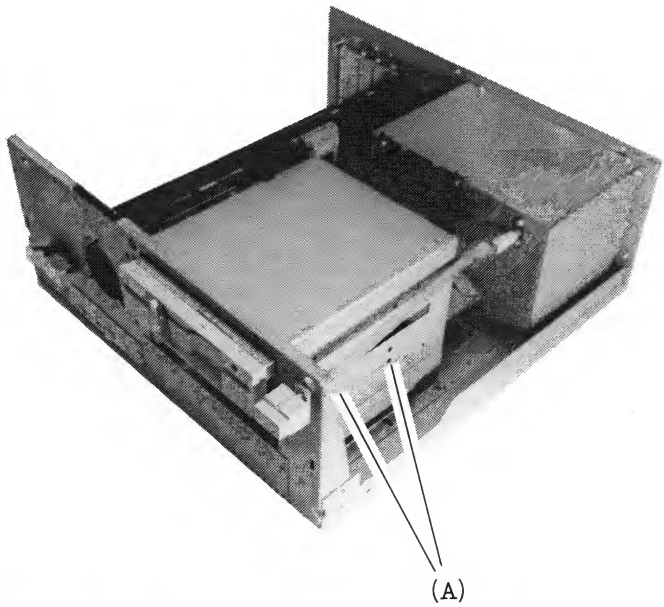


FIGURE 5-9. DISK DRIVE UNIT REMOVAL/REPLACEMENT

5.2.18 DISK DRIVE UNIT (FDD OR HDD) REPLACEMENT

Refer to Figure 5-9 above.

1. Slide the drive unit through the opening in the front case, and secure the drive unit with two screws (A).
2. Connect the cables to the drive unit.
3. Replace the cover. (Refer to Section 5.2.2)

5.3 POWER SUPPLY (ADRPS) UNIT

The following pages describe and illustrate the procedures to be used for the removal and the replacement of components of the power supply unit.

5.3.1 POWER SUPPLY COVER REMOVAL

Refer to Figure 5 – 10 below.

1. Remove the four screws (labeled A).
2. Disconnect the fan connector (labeled B), and remove the cover (labeled C).

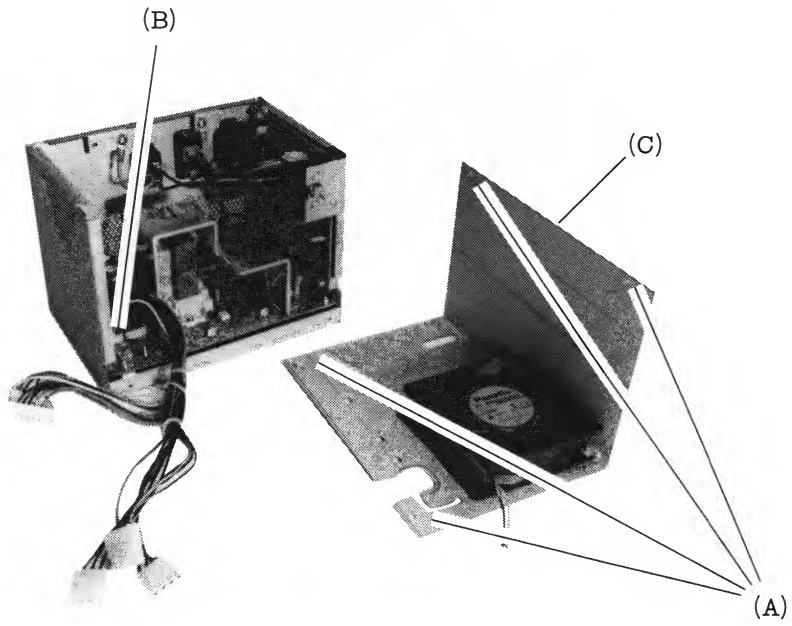


FIGURE 5 – 10. COVER REMOVAL/REPLACEMENT

5.3.2 COVER REPLACEMENT

Refer to Figure 5 – 10 above.

1. Connect the connector (B), and fasten the cover with four screws (A).
2. Fasten the DC cables to the cover (C) using cable clamps.

5.3.3 AC FILTER BOARD REMOVAL

Refer to Figure 5 – 11 below.

1. Remove the cover. (Refer to Section 5.3.1)
2. Remove the three screws (labeled A), and disconnect the three connectors (labeled B).
3. Remove the five screws (labeled C) fastening the AC filter board.
4. Remove the solder fixing the two jumper cables (labeled D) on the AC filter board, and remove the AC filter board.

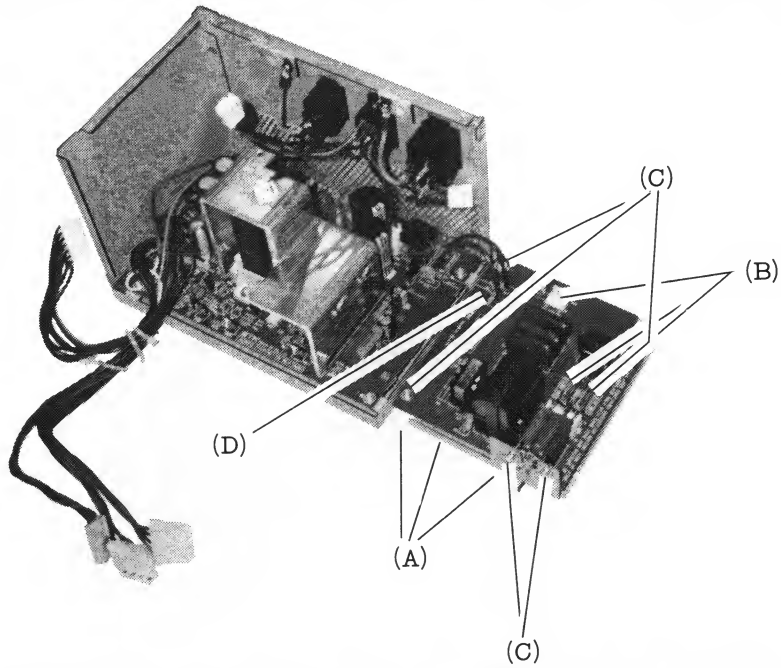


FIGURE 5 – 11. AC FILTER BOARD REMOVAL/REPLACEMENT

5.3.4 AC FILTER BOARD REPLACEMENT

Refer to Figure 5 – 11 above.

1. Solder the two jumper cables (D) to the AC filter board.
2. Secure the five screws (C).
3. Connect the three connectors (A). (CN6 on the AC filter board < – – – > AC voltage select switch, CN8 on the AC filter board < – – – > AC inlet)
4. Secure the three screws (A).
5. Replace the cover. (Refer to Section 5.3.2)

5.3.5 DC MAIN BOARD REMOVAL

Refer to Figure 5 – 12 below.

1. Remove the cover. (Refer to Section 5.3.1)
2. Remove the three screws (labeled A).
3. Disconnect the three connectors (labeled B) on the AC filter board.
4. Remove the five screws (labeled C) fastening the DC main board to case, and disconnect the connector labeled (D).
5. Remove the solder fixing the two jumper cables (labeled E) on the DC main board, and remove the DC main board.

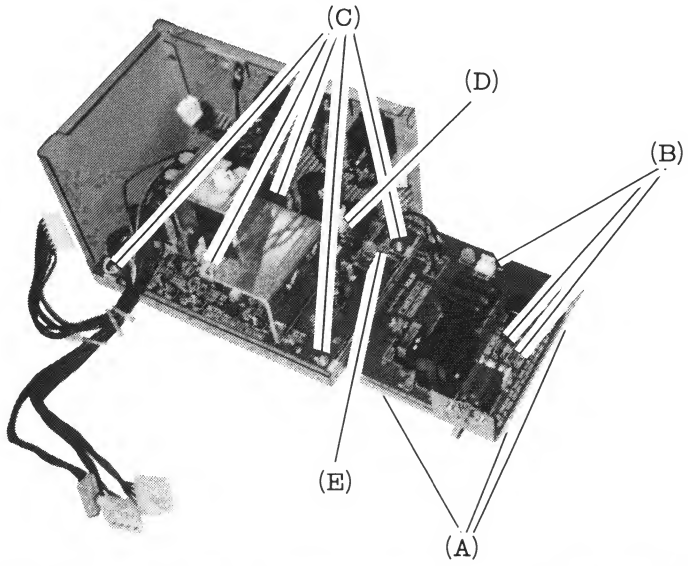


FIGURE 5 – 12. DC MAIN BOARD REMOVAL/REPLACEMENT

5.3.6 DC MAIN BOARD REPLACEMENT

Refer to Figure 5 – 12 above.

1. Solder the two jumper cables (D) to the DC main board.
2. Replace and tighten the five screws (B) to fasten the DC main board, and connect the connector labeled (C).
3. Connect the three connectors (A) to the AC filter board. (CN6 on the AC filter board < – – – > AC voltage select switch, CN8 on the AC filter board < – – – > AC outlet)
4. Replace and tighten the three screws (B) to fasten the AC filter board to the case.
5. Replace the cover. (Refer to Section 5.3.2)

CHAPTER 6

ADJUSTMENTS AND MAINTENANCE

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A.1 JUMPER SETTINGS

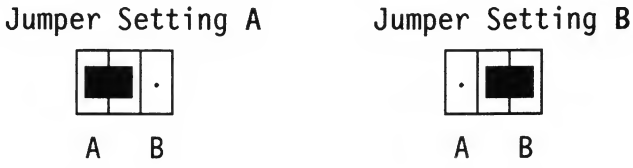


FIGURE A – 1. JUMPER SETTINGS

TABLE A – 1. SYSTEM BOARD JUMPERS

Jumper No. 1	2	3	4	5	Functional Description
			A	A	NPX Clock Speed = 8MHz (high-speed mode)
			A	B	(Prohibited)
			B	A	(Prohibited)
			B	B	NPX Clock = 2/3 CPU Clock speed
	B	B			4 Wait Cycles for 16-bit Expansion Bus DRAM
	A	B			3 Wait Cycles for 16-bit Expansion Bus DRAM
	B	A			2 Wait Cycles for 16-bit Expansion Bus DRAM
	A	A			1 Wait Cycle for 16-bit Expansion Bus DRAM
A					1 Wait Cycle for EPROM Access
B					2 Wait Cycles for EPROM Access

Note: Selectable wait cycles apply only to 10 MHz operation.

TABLE A – 2. SYSTEM MEMORY CARD JUMPERS

Jumper 1	2	3	Functional Description
A	A		640K Bytes of RAM Enabled
B	A		512K Bytes of RAM Enabled (Upper 128K Disabled)
A	B		(Not used)
B	B		256K Bytes of RAM Enabled (Upper 256K Disabled)
		A	27128 EPROM Size
		B	27256 EPROM Size

TABLE A-3. EPSON MULTI-FUNCTION BOARD JUMPERS

Jumper Number 10	9	6	5	4	3	Functional Description
A				A	A	Parallel Port Enabled as Primary
B				B	A	Parallel Port Enabled as Secondary
A				A	B	Compatible w/IBM Monochrome Adapter
x				B	B	Parallel Port Disabled
	A	A	A			Serial Port Enabled as Primary
	B	B	A			Serial Port Enabled as Secondary
	x	x	B			Serial Port Disabled

x = Don't Care

A.2 PIN ASSIGNMENT OF CONNECTORS

The interconnections of the system unit, keyboard, monitor, and all boards are summarized in Table A – 4 through A – 7. Pin assignments for each connector are detailed in section A.2.1 through A.2.4.

TABLE A – 4. CONNECTOR SUMMARY OF ANDRO BOARD UNIT

CONNECTOR	*TYPE*	*DESCRIPTION*	*REFERENCE*
CN1	H421023 – 31	I/O CHANNEL FOR OPTION	A.2.1.1
CN2	H421023 – 31	I/O CHANNEL FOR OPTION	A.2.1.1
CN3	H421023 – 52 – 11	I/O CHANNEL FOR OPTION	A.2.1.1
CN4	H421023 – 52 – 11	I/O CHANNEL FOR OPTION	A.2.1.1
CN5	H421023 – 52 – 11	I/O CHANNEL FOR OPTION	A.2.1.1
CN6	H421023 – 52 – 11	I/O CHANNEL FOR OPTION	A.2.1.1
CN6	H421023 – 31	I/O CHANNEL FOR OPTION	A.2.1.1
CN7	PCN10C – 64S – 2.54DSA	SYSTEM MEMORY CARD	A.2.1.2
CN8	00 – 8283 – 0212 – 00 – 0000	SPEAKER I/F	A.2.1.3
CN9	IL – 2P – – S3EN2	BATTERY (6V)	A.2.1.4
CN10	00 – 8263 – 0312 – 00 – 0000	LED (POWER/CPU SPEED)	A.2.1.5
CN11	B5B – XH – A	KEYBOARD I/F	A.2.1.6
CN12	B5P – VH	POWER SUPPLY (1)	A.2.1.7
CN13	B7P – VH	POWER SUPPLY (2)	A.2.1.8

TABLE A – 5. CONNECTOR SUMMARY OF SPF2 BOARD UNIT

CONNECTOR	*TYPE*	*DESCRIPTION*	*REFERENCE*
CN1	GMM – X9UGDMDB1	EXTERNAL SERIAL DEVICE I/F	A.2.2.1
CN2	9MM – X25UGDFDB1	EXTERNAL PARALLEL PRINTER I/F	A.2.2.2
CN3	7634 – 5002 SC	TWO INTERNAL FDDS I/F (DRIVE A:, B:)	A.2.2.3

TABLE A – 6. CONNECTOR SUMMARY OF ADR – RM3 BOARD UNIT

CONNECTOR	*TYPE*	*DESCRIPTION*	*REFERENCE*
CN1	PCN10A – 64A – 2.54DS	I/O CONNECTION TO MAIN CPU UNIT	A.2.3.1
CN2	A1 – 34PA – 2.54DSA	CONNECTION WITH SEMI MEMORY CARD	A.2.3.3
CN3	A1 – 6PA – 2.54DSA	POWER SUPPLY FOR SEMI MEMORY CARD	A.2.3.3

TABLE A – 7. CONNECTOR SUMMARY OR ADR – RM3S BOARD UNIT

CONNECTOR	*TYPE*	*DESCRIPTION*	*REFERENCE*
CN1	HIF3H – 34DA – 2.54DSA	CONNECTION WITH MAIN MEMORY CARD	A.2.4.1
CN2	HIF3H06DA – 2.54DSA	POWER SUPPLY FROM ADR – RM3	A.2.4.2

A.2.1 ANDRO BOARD

A.2.1.1 CONNECTOR CN1 THROUGH CN6

Use : I/O channel for option card
Type : H421023 – 31 (CN1, 2, 6)
H421023 – 52 – 11 (CN3, 4, 5)

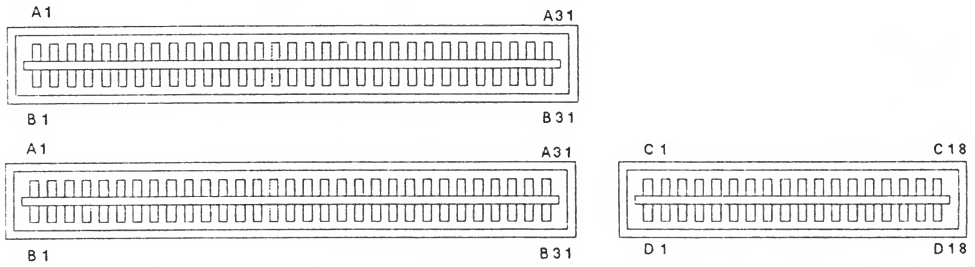


FIGURE A – 2. CN1 THROUGH CN6 PIN LOCATIONS

TABLE A – 8. CN1 THROUGH CN6 PIN ASSIGNMENT (A – SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
A1	– I/O CH CK	I	I/O channel check
A2	SD7	I/O	System Data Bit 7
A3	SD6	I/O	System Data Bit 6
A4	SD5	I/O	System Data Bit 5
A5	SD4	I/O	System Data Bit 4
A6	SD3	I/O	System Data Bit 3
A7	SD2	I/O	System Data Bit 2
A8	SD1	I/O	System Data Bit 1
A9	SD0	I/O	System Data Bit 0
A10	+ I/O CH RDY	I	I/O channel Ready
A11	AEN	O	Address Latch Enable
A12	SA19	I/O	System Address Bit 19
A13	SA18	I/O	System Address Bit 18
A14	SA17	I/O	System Address Bit 17
A15	SA16	I/O	System Address Bit 16
A16	SA15	I/O	System Address Bit 15
A17	SA14	I/O	System Address Bit 14
A18	SA13	I/O	System Address Bit 13
A19	SA12	I/O	System Address Bit 12
A20	SA11	I/O	System Address Bit 11
A21	SA10	I/O	System Address Bit 10
A22	SA9	I/O	System Address Bit 9
A23	SA8	I/O	System Address Bit 8
A24	SA7	I/O	System Address Bit 7
A25	SA6	I/O	System Address Bit 6
A26	SA5	I/O	System Address Bit 5
A27	SA4	I/O	System Address Bit 4

TABLE A-8. (Continued)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
A28	SA3	I/O	System Address Bit 3
A29	SA2	I/O	System Address Bit 2
A30	SA1	I/O	System Address Bit 1
A31	SA0	I/O	System Address Bit 0

TABLE A-9. CN1 THROUGH CN6 PIN ASSIGNMENT (B-SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
B1	GND	–	Ground
B2	RESET DRV	O	Reset Driver
B3	+5VDC	–	+5V DC
B4	IRQ9	I	Interrupt Request 9
B5	-5VDC	–	-5V DC
B6	DRQ2	I	DMA Request 2
B7	-12VDC	–	+12V DC
B8	0WS	I	Wait Indication Signal
B9	+12VDC	–	+12V DC
B10	GND	–	Ground
B11	-SMEMW	O	System Memory Write Signal Comand
B12	-SMEMR	O	System Memory Read Signal Command
B13	-IOW	I/O	I/O Write Command
B14	-IOR	I/O	I/O Read Command
B15	-DACK3	O	DMA Acknowledge 3
B16	DRQ3	I	DMA Request 3
B17	-DACK3	0	DMA Acknowledge 1
B18	DRQ1	I	DMA Request 1
B19	-Refresh	I/O	Refresh Signal
B20	CLK	O	System Clock
B21	IRQ7	I	Interrupt Request 7
B22	IRQ6	I	Interrupt Request 6
B23	IRQ5	I	Interrupt Request 5
B24	IRQ4	I	Interrupt Request 4
B25	IRQ3	I	Interrupt Request 3
B26	-DACK2	O	DMA Acknowledge 2
B27	T/C	O	Terminal Count
B28	BALE	O	Bus Address Latch Enable
B29	+5VDC	–	+5V DC
B30	OSC	O	Oscillator
B31	GND	–	Ground

TABLE A – 10. CN1, CN2, CN6 PIN ASSIGNMENT (C – SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
C1	SBHE	I/O	System Bus High Enable
C2	LA23	I/O	Unlatched System Address Bit 23
C3	LA22	I/O	Unlatched System Address Bit 22
C4	LA21	I/O	Unlatched System Address Bit 21
C5	LA20	I/O	Unlatched System Address Bit 20
C6	LA19	I/O	Unlatched System Address Bit 19
C7	LA18	I/O	Unlatched System Address Bit 18
C8	LA17	I/O	Unlatched System Address Bit 17
C9	– MEMR	O	System Memory Read Signal
C10	– MEMW	O	System Memory Write Signal
C11	SD8	I/O	System Data Bit 8
C12	SD9	I/O	System Data Bit 9
C13	SD10	I/O	System Data Bit 10
C14	SD11	I/O	System Data Bit 11
C15	SD12	I/O	System Data Bit 12
C16	SD13	I/O	System Data Bit 13
C17	SD14	I/O	System Data Bit 14
C18	SD15	I/O	System Data Bit 15

TABLE A – 11. CN1, CN2, CN6 PIN ASSIGNMENT (D – SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
D1	– MEM CS16	I	Chip Select Signal of 16bits Memory
D2	– I/O CS16	I	Chip Select Signal of 16bits I/O
D3	IRQ10	I	Interrupt Request 10
D4	IRQ11	I	Interrupt Request 11
D5	IRQ12	I	Interrupt Request 12
D6	IRQ13	I	Interrupt Request 13
D7	IRQ14	I	Interrupt Request 14
D8	– DACK0	O	DMA Acknowledge 0
D9	DRQ0	I	DMA Request 0
D10	– DACK5	O	DMA Acknowledge 5
D11	DRQ5	I	DMA Request 5
D12	– DACK6	O	DMA Acknowledge 6
D13	DRQ6	I	DMA Request 6
D14	– DACK7	O	DMA Acknowledge 7
D15	DRQ7	I	DMA Request 7
D16	+5 VDC	–	+5V DC
D17	– MASTER	I	Direction Control of CPU Address Bus (A23 – 17)
D18	GND	–	Ground

A.2.1.2 CONNECTOR CN7

Use : System Memory Card
Type : PCN10C – 64S – 2. 54DSA

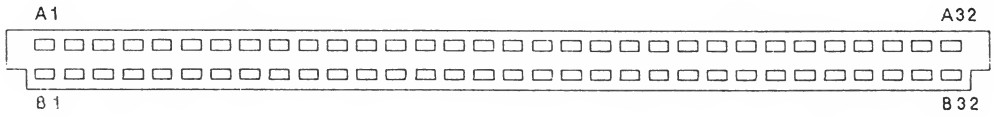


FIGURE A – 3. CN7 PIN LOCATIONS

TABLE A – 12. CN7 PIN ASSIGNMENT (A – SIDE)

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
A1	+5VDC	–	+5V DC
A2	– LMGCS	I	Enable Control of SMWN and SMRN
A3	– CSROM	I	Chip Select Signal of Internal ROM
A4	– CSRAM	I	Chip Select Signal of Internal RAM
A5	– XMEMW	O	Internal Memory Write Signal
A6	– XMEMR	O	Internal Memory Read Signal
A7	– MEMR	O	System Memory Read Signal
A8	– MEMW	O	System Memory Write Signal
A9	– XBHE	O	Internal Bus High Enable
A10	HLDA	O	Hold Acknowledge
A11	ALE	O	Address Latch Enable
A12	DMD	I	Direction Control of Memory Data Bus
A13	– RF2D	O	Refresh Signal
A14	– REFSH	O	Refresh Signal
A15	MD0	I/O	Memory Data Bit 0
A16	MD1	I/O	Memory Data Bit 1
A17	MD2	I/O	Memory Data Bit 2
A18	MD3	I/O	Memory Data Bit 3
A19	MD4	I/O	Memory Data Bit 4
A20	MD5	I/O	Memory Data Bit 5
A21	MD6	I/O	Memory Data Bit 6
A22	MD7	I/O	Memory Data Bit 7
A23	MD8	I/O	Memory Data Bit 8
A24	MD9	I/O	Memory Data Bit 9
A25	MD10	I/O	Memory Data Bit 10
A26	MD11	I/O	Memory Data Bit 11

TABLE A – 12. (Continued)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
A27	MD12	I/O	Memory Data Bit 12
A28	MD13	I/O	Memory Data Bit 13
A29	MD14	I/O	Memory Data Bit 14
A30	MD15	I/O	Memory Data Bit 15
A31	+5 VDC	–	+5V DC
A32	GND	–	Ground

TABLE A – 13. CN7 PIN ASSIGNMENT (B – SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
B1	GND	–	Ground
B2	JRAM	O	Enable Control of DRAM
B3	ENPR	O	Enable RAM Parity Check
B4	– PCK	I	Parity Check Error
B5	SA0	I/O	System Address Bit 0
B6	SA1	I/O	System Address Bit 1
B7	SA2	I/O	System Address Bit 2
B8	SA3	I/O	System Address Bit 3
B9	SA4	I/O	System Address Bit 4
B10	SA5	I/O	System Address Bit 5
B11	SA6	I/O	System Address Bit 6
B12	SA7	I/O	System Address Bit 7
B13	SA8	I/O	System Address Bit 8
B14	SA9	I/O	System Address Bit 9
B15	SA10	I/O	System Address Bit 10
B16	SA11	I/O	System Address Bit 11
B17	SA12	I/O	System Address Bit 12
B18	SA13	I/O	System Address Bit 13
B19	SA14	I/O	System Address Bit 14
B20	SA15	I/O	System Address Bit 15
B21	SA16	I/O	System Address Bit 16
B22	SA17	I/O	System Address Bit 17
B23	SA18	I/O	System Address Bit 18
B24	A17	O	CPU Address Bit 17
B25	A18	O	CPU Address Bit 18
B26	A19	O	CPU Address Bit 19
B27	A20	O	CPU Address Bit 20
B28	A21	O	CPU Address Bit 21
B29	A22	O	CPU Address Bit 22
B30	A23	O	CPU Address Bit 23
B31	+5 VDC	–	+5V DC
B32	GND	–	Ground

A.2.1.3 CONNECTOR CN8

Use : Speaker Interface
Type : 00 – 8283 – 0212 – 00 – 0000

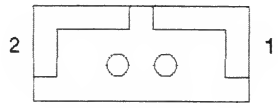


FIGURE A – 4. CN8 PIN LOCATIONS

TABLE A – 14. CN8 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	SP +	I	Speaker Frequency
2	SP –	–	Speaker Ground

A.2.1.4 CONNECTOR CN9

Use : Battery (6V)
Type : IL – 2P – – S3EN2

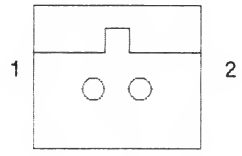


FIGURE A – 5. CN9 PIN LOCATIONS

TABLE A – 15. CN9 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	GND	–	Ground
2	6V	–	Battery Back Up

A.2.1.5 CONNECTOR CN10

Use : LED (CPU Speed)
Type : 00 – 8263 – 0312 – 00 – 0000

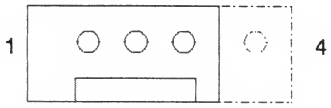


FIGURE A – 6. CN10 PIN LOCATIONS

TABLE A – 16. CN10 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	GND	–	Ground
2	GREEN	–	Clock 8MHz
3	RED	–	Clock 10MHz
4	NC	–	No Connection

A.2.1.6 CONNECTOR CN11

Use : Keyboard Interface
Type : B5B – XH – A

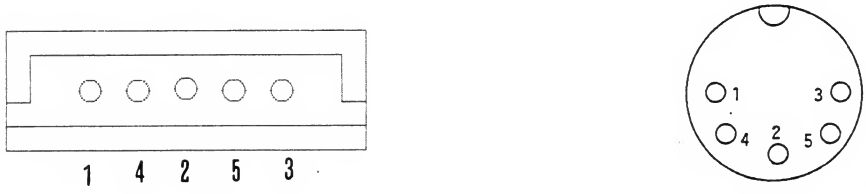


FIGURE A – 7. CN11 PIN LOCATIONS

TABLE A – 17. CN11 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	KBD CLK	I/O	Keyboard Clock
2	KBD DATA	I/O	Keyboard Data
3	KEY	–	No Connection
4	GND	–	Ground
5	Vcc	–	Power

A.2.1.7 CONNECTOR CN12

Use : Power Supply (1)
Type : B5P – VH

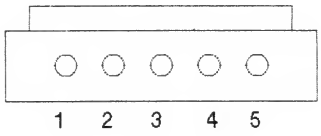


FIGURE A – 8. CN12 PIN LOCATIONS

TABLE A – 18. CN12 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	POWER DOWN	I	Power Down Signal
2	+5V	–	+5V DC
3	+12V	–	+12V DC
4	–12V	–	–12V DC
5	GL	–	Ground

A.2.1.8 CONNECTOR CN13

Use : Power Supply (2)
Type : B7P – VH

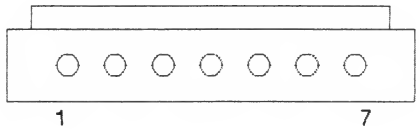


FIGURE A – 9. CN13 PIN LOCATIONS

TABLE A – 19. CN13 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	GL	–	Ground
2	GL	–	Ground
3	GL	–	Ground
4	– 5V	–	– 5V DC
5	+ 5V	–	+ 5V DC
6	+ 5V	–	+ 5V DC
7	+ 5V	–	+ 5V DC

A.2.2 SPF2 BOARD

A.2.2.1 CONNECTOR CN1

Use : External Serial Device Interface
Type : GMM-X9 UGDMDB1

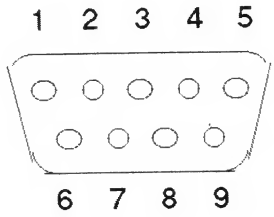


FIGURE A-10. CN1 PIN LOCATIONS

TABLE A-20. CN1 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	CRDET	I	Data Carrier Detect
2	RXDT	I	Receive Data
3	TXDT	O	Transmit Data
4	DTR	O	Data Terminal Ready
5	SG	–	Signal Ground
6	DSR	I	Data Set Ready
7	RTS	O	Request to Serial
8	CTS	I	Clear to Send
9	RI	I	Ring Indicator

A.2.2.2 CONNECTOR CN2

Use : External Parallel Printer Interface
Type : GMM – 25 UGDFDB1

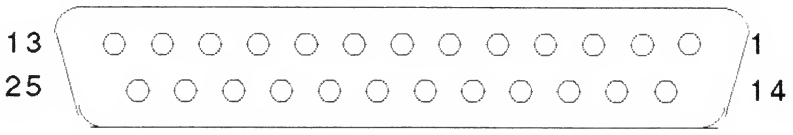


FIGURE A – 11. CN2 PIN LOCATIONS

TABLE A – 21. CN2 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	– STROBE	O	
2	DATA0	O	Printer Data Bit 0
3	DATA1	O	Printer Data Bit 1
4	DATA2	O	Printer Data Bit 2
5	DATA3	O	Printer Data Bit 3
6	DATA4	O	Printer Data Bit 4
7	DATA5	O	Printer Data Bit 5
8	DATA6	O	Printer Data Bit 6
9	DATA7	O	Printer Data Bit 7
10	– ACK	I	Acknowledge
11	+ BUSY	I	Printer Busy
12	+ PE	I	End of Paper
13	+ SLCT	I	Printer Select
14	– AUTOFT	I	Auto Feed
15	– ERROR	I	Printer Error
16	– INIT	I	Printer Initialize
17	– SLCTIN	I	Printer Select 12
18	GND	–	Ground
19	GND	–	Ground
20	GND	–	Ground
21	GND	–	Ground
22	GND	–	Ground
23	GND	–	Ground
24	GND	–	Ground
25	GND	–	Ground

A.2.2.3 CONNECTOR CN3

Use : Two Internal FDDs Interface
Type : 7634 – 5002 SC

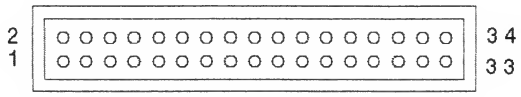


FIGURE A – 12 CN3 PIN LOCATIONS

TABLE A – 22. CN3 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
Odd Pin	GND	–	Ground
2	– RWC	O	High/Normal Density
4	NC	–	No connection
6	NC	–	No connection
8	– INDEX	I	Index
10	– MOT1	O	Motor Enable 1
12	– DS1	O	Driver Select 2
14	– DS1	O	Driver Select 1
16	– MOT2	O	Motor Enable 2
18	– DIRS	O	Direction
20	– STEP	O	Step
22	– WDATA	O	Writer Date
24	– wen	O	Write Enable
26	– TRK0	I	Track 00
28	– WPRT	I	Write Protect
30	– RDATA	I	Read Data
32	– SIDE	O	Head Select
34	– DSKCHG	I	Disk Change

A.2.3 ADR – RM3 BOARD

A.2.3.1 CONNECTOR CN1

Use : I/O Connector to Main CPU Unit
Type : PCN/OA – 64A – 2.5DS

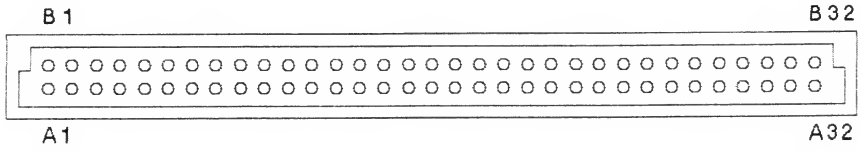


FIGURE A – 13. CN1 PIN LOCATIONS

TABLE A – 23. CN1 PIN ASSIGNMENT (A – SIDE)

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
A1	+5VDC	–	+5V DC
A2	– LMGCS	O	Enable Control of SMWN and SMRN
A3	– CSROM	O	Chip Select Signal of Internal ROM
A4	– CSRAM	O	Chip Select Signal of Internal RAM
A5	– XMEMW	I	Internal Memory Write Signal
A6	– XMEMR	I	Internal Memory Read Signal
A7	– MEMR	I	System Memory Read Signal
A8	– MEMW	I	System Memory Write Signal
A9	– XBHE	I	Internal Bus High Enable
A10	HLDA	I	Hold Acknowledge
A11	ALE	I	Address Latch Enable
A12	DMD	O	Direction Ctl of Memory Data Bus
A13	– RF2D	I	Refresh Signal
A14	– REFSH	I	Refresh Signal
A15	MD0	I/O	Memory Data Bit 0
A16	MD1	I/O	Memory Data Bit 1
A17	MD2	I/O	Memory Data Bit 2
A18	MD3	I/O	Memory Data Bit 3
A19	MD4	I/O	Memory Data Bit 4
A20	MD5	I/O	Memory Data Bit 5
A21	MD6	I/O	Memory Data Bit 6
A22	MD7	I/O	Memory Data Bit 7
A23	MD8	I/O	Memory Data Bit 8
A24	MD9	I/O	Memory Data Bit 9
A25	MD10	I/O	Memory Data Bit 10
A26	MD11	I/O	Memory Data Bit 11

TABLE A-23. (Continued)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
A27	MD12	I/O	Memory Data Bit 12
A28	MD13	I/O	Memory Data Bit 13
A29	MD14	I/O	Memory Data Bit 14
A30	MD15	I/O	Memory Data Bit 15
A31	+5VDC	-	+5V DC
A32	GND	-	Ground

* This pin assignment is compatible with the ANDRO CN7. (A.2.1.2)

TABLE A-24. CN1 PIN ASSIGNMENT (B-SIDE)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
B1	GND	-	Ground
B2	JRAM	I	Enable Control of DRAM
B3	ENPR	I	Enable RAM Parity Check
B4	-PCK	O	Parity Check Error
B5	SA0	I/O	System Address Bit 0
B6	SA1	I/O	System Address Bit 1
B7	SA2	I/O	System Address Bit 2
B8	SA3	I/O	System Address Bit 3
B9	SA4	I/O	System Address Bit 4
B10	SA5	I/O	System Address Bit 5
B11	SA6	I/O	System Address Bit 6
B12	SA7	I/O	System Address Bit 7
B13	SA8	I/O	System Address Bit 8
B14	SA9	I/O	System Address Bit 9
B15	SA10	I/O	System Address Bit 10
B16	SA11	I/O	System Address Bit 11
B17	SA12	I/O	System Address Bit 12
B18	SA13	I/O	System Address Bit 13
B19	SA14	I/O	System Address Bit 14
B20	SA15	I/O	System Address Bit 15
B21	SA16	I/O	System Address Bit 16
B22	SA17	I/O	System Address Bit 17
B23	SA18	I/O	System Address Bit 18
B24	A17	I	CPU Address Bit 17
B25	A18	I	CPU Address Bit 18
B26	A19	I	CPU Address Bit 19
B27	A20	I	CPU Address Bit 20
B28	A21	I	CPU Address Bit 21
B29	A22	I	CPU Address Bit 22
B30	A23	I	CPU Address Bit 23
B31	+5VDC	-	+5V DC
B32	GND	-	Ground

* This pin assignment is compatible with the ANDRO CN7 (A.2.1.2) except the direction of the signal.

A.2.3.2 CONNECTOR CN2

Use : Connection with Semi – Memory Card
Type : A1 – 34PA – 2.54DSA

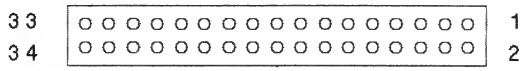


FIGURE A – 14. CN2 PIN LOCATIONS

TABLE A – 25. CN2 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
1	GND	–	Ground
2	+5V	–	+5V (Power)
3	– WE	O	Write Enable Signal for DRAM
4	– CASL	O	Column Address Strobe for Even Byte
5	– CASH	O	Column Address Strobe for Odd Byte
6	– RAS0	O	Row Address Strobe
7	MA0	O	DRAM Address Bit 0
8	MA1	O	DRAM Address Bit 1
9	MA2	O	DRAM Address Bit 2
10	MA3	O	DRAM Address Bit 3
11	MA4	O	DRAM Address Bit 4
12	MA5	O	DRAM Address Bit 5
13	MA6	O	DRAM Address Bit 6
14	MA7	O	DRAM Address Bit 7
15	MA8	O	DRAM Address Bit 8
16	MD0	I	Memory Data Bit 0
17	GND	–	Ground
18	MD1	I	Memory Data Bit 1
19	MD2	I	Memory Data Bit 2
20	MD3	I	Memory Data Bit 3
21	MD4	I	Memory Data Bit 4
22	MD5	I	Memory Data Bit 5
23	MD6	I	Memory Data Bit 6
24	MD7	I	Memory Data Bit 7
25	MD8	I	Memory Data Bit 8

TABLE A – 25. (Continued)

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
26	MD9	I	Memory Data Bit 9
27	MD10	I	Memory Data Bit 10
28	MD11	I	Memory Data Bit 11
29	MD12	I	Memory Data Bit 12
30	MD13	I	Memory Data Bit 13
31	MD14	I	Memory Data Bit 14
32	MD15	I	Memory Data Bit 15
33	GND	–	Ground
34	+5V	–	+5V (Power)

A.2.3.3 CONNECTOR CN3

Use : Power Supply for Semi – Memory Card
Type : A1 – 6PA – 2.54DSA

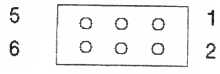


FIGURE A – 15. CN3 PIN LOCATIONS

TABLE A – 26. CN3 PIN ASSIGNMENT

PIN NO.	*SIGNAL NAME*	*DIRECTION*	*DESCRIPTION*
Even Pin	+5V	–	+5V (Power)
Odd Pin	GND	–	Ground

A.2.4 ADR – RM3S BOARD

A.2.4.1 CONNECTOR CN1

Use : Connection with Main – Memory Card
Type : HIF3H – 34DA – 2.54DSA

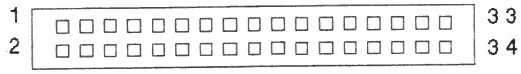


FIGURE A – 16. CN1 PIN LOCATIONS

TABLE A – 27. CN1 PIN ASSIGNMENT

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
1	GND	–	Ground
2	+5V	–	+5V (Power)
3	– WE	O	Write Enable Signal for DRAM
4	– CASL	O	Column Address Strobe for Even Byte
5	– CASH	O	Column Address Strobe for Odd Byte
6	– RAS0	O	Row Address Strobe
7	MA0	O	DRAM Address Bit 0
8	MA1	O	DRAM Address Bit 1
9	MA2	O	DRAM Address Bit 2
10	MA3	O	DRAM Address Bit 3
11	MA4	O	DRAM Address Bit 4
12	MA5	O	DRAM Address Bit 5
13	MA6	O	DRAM Address Bit 6
14	MA7	O	DRAM Address Bit 7
15	MA8	O	DRAM Address Bit 8
16	MD0	I	Memory Data Bit 0
17	GND	–	Ground
18	MD1	I	Memory Data Bit 1
19	MD2	I	Memory Data Bit 2
20	MD3	I	Memory Data Bit 3
21	MD4	I	Memory Data Bit 4
22	MD5	I	Memory Data Bit 5
23	MD6	I	Memory Data Bit 6
24	MD7	I	Memory Data Bit 7
25	MD8	I	Memory Data Bit 8
26	MD9	I	Memory Data Bit 9

TABLE A – 27. (Continued)

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
27	MD10	I	Memory Data Bit 10
28	MD11	I	Memory Data Bit 11
29	MD12	I	Memory Data Bit 12
30	MD13	I	Memory Data Bit 13
31	MD14	I	Memory Data Bit 14
32	MD15	I	Memory Data Bit 15
33	GND	–	Ground
34	+5V	–	+5V (Power)

A.2.4.2 CONNECTOR CN2

Use : Power Supply for Main Memory Card
Type : HIF3H – 6DA – 2.54DSA

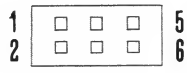


FIGURE A – 17. CN2 PIN LOCATIONS

TABLE A – 28. CN2 PIN ASSIGNMENT

PIN NO.	SIGNAL NAME	DIRECTION	DESCRIPTION
Even Pin	+5V	–	+5V (Power)
Odd Pin	GND	–	Ground

LIST OF DIAGRAMS

LIST OF DIAGRAMS

THIS SIZE IS A1.
DRAWN BY M1N1.

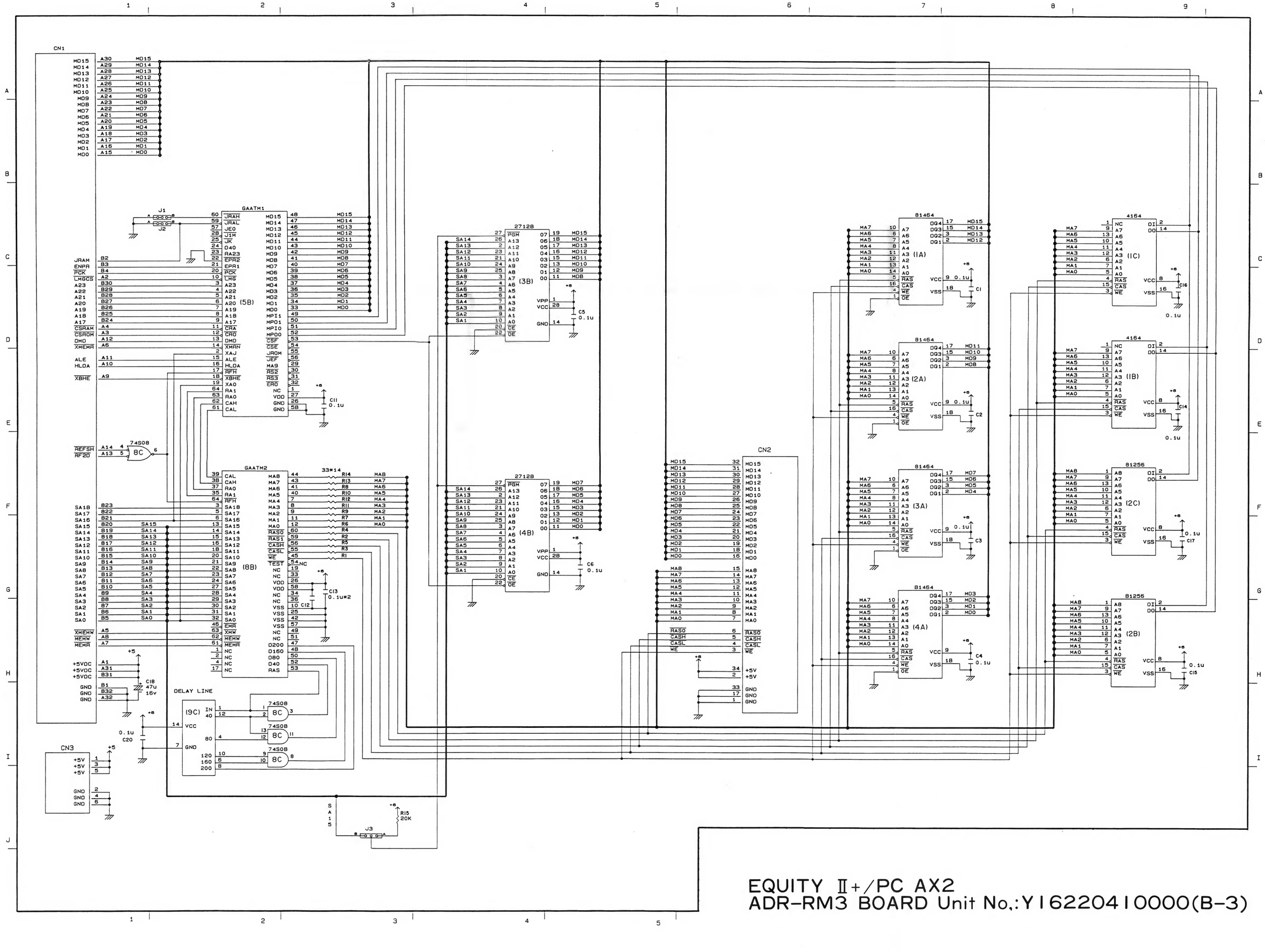
EQUITY Ⅱ+/EPSON PC AX2
ANDRO BOARD Unit No,:Y1622010000(B-1)

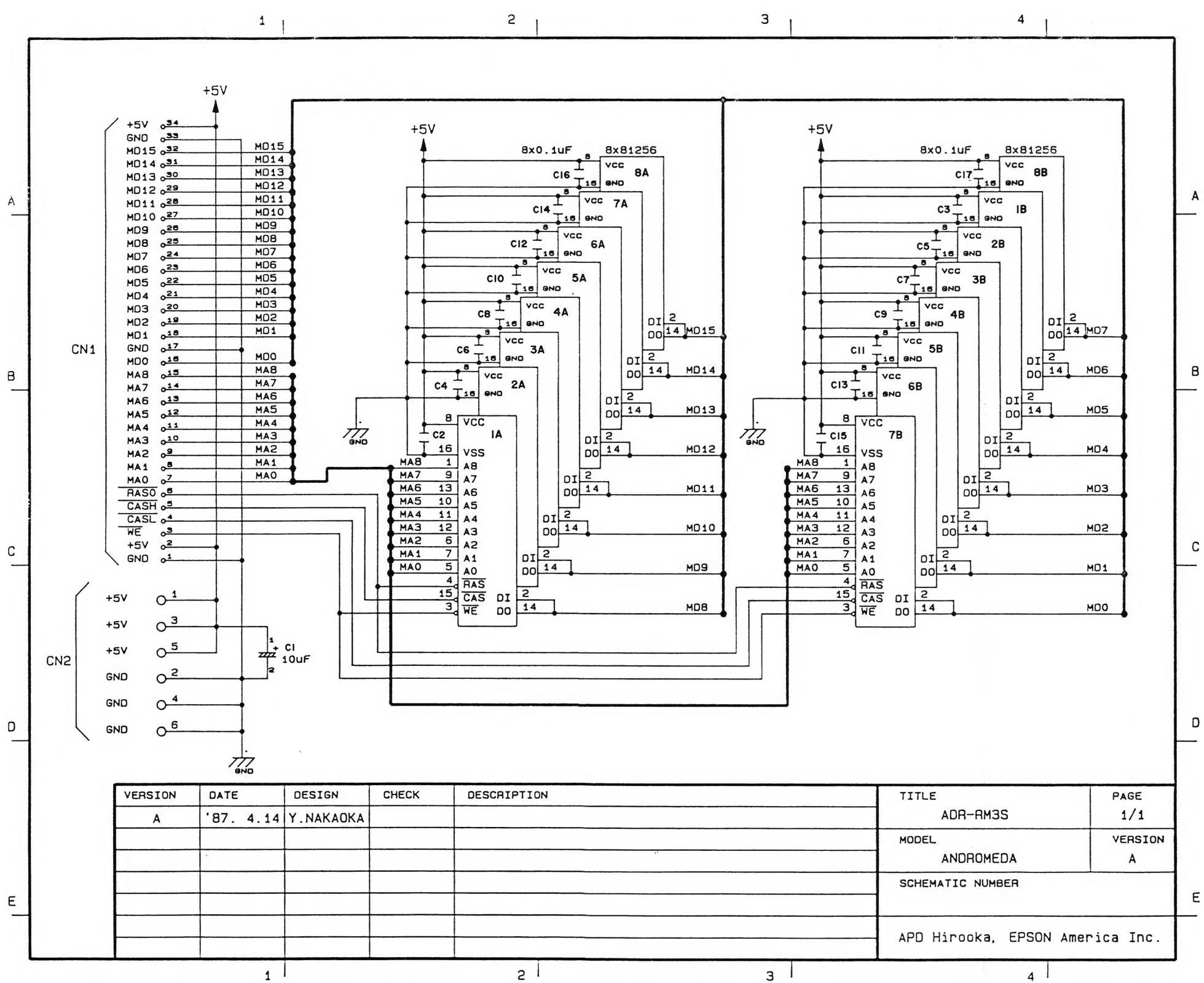
GRID 10,10 FOR BORDER.
GRID 5,5 FOR LOGICAL SYMBOLS.

THIS SIZE IS A1.
DRAWN BY MiNi.

EQUITY II+/EPSON PC AX2
SPF II BOARD Unit No.:Y1622030000(B-2)

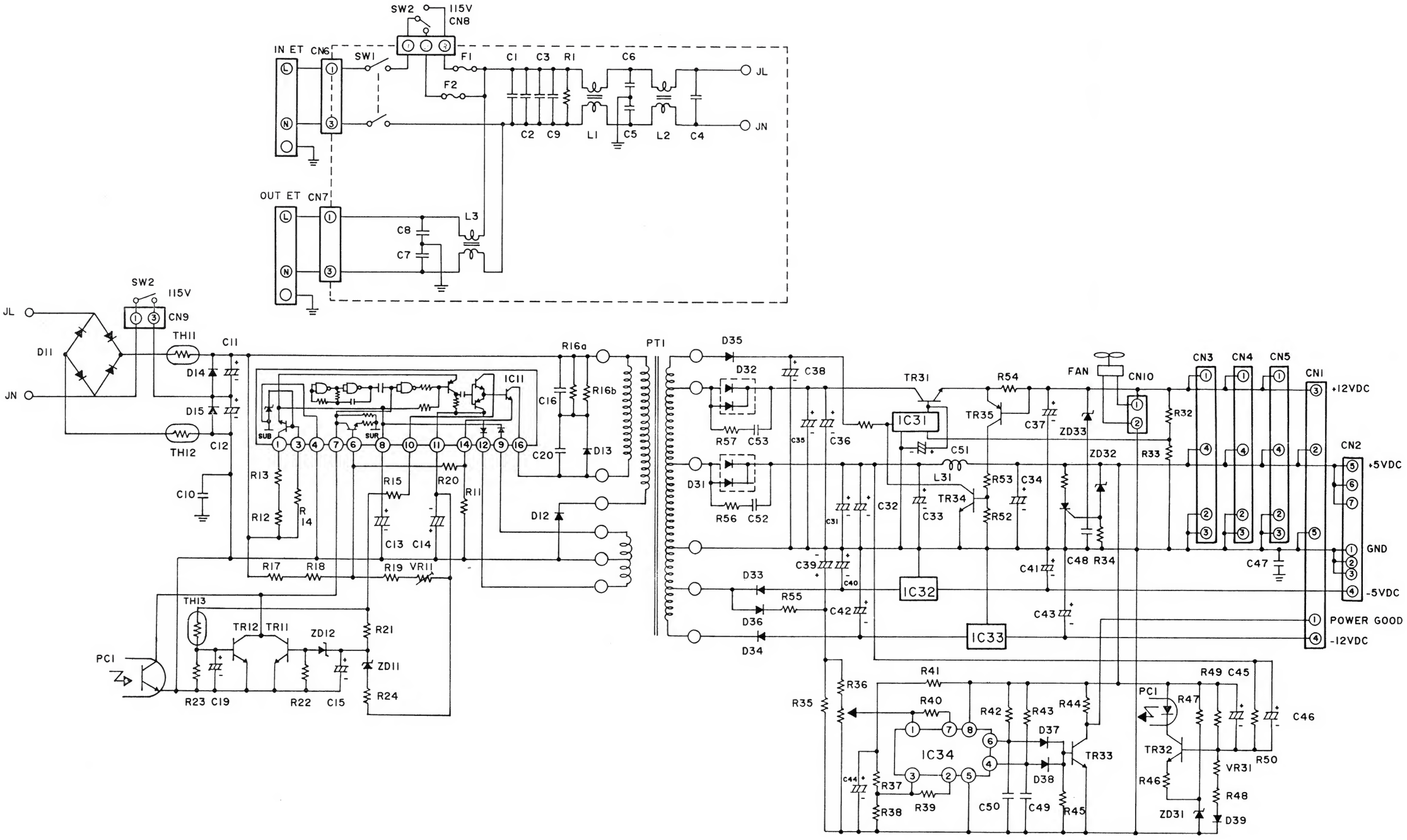
GRID 10.10 FOR BORDER.
GRID 5.5 FOR LOGICAL SYMBOLS.


CN1
GAATM1
GAATM2
(5B)
(8B)
(9C)
27128
(3B)
(4B)
74S08
8C
DELAY LINE
CN2
CN3
81464
(1A)
(2A)
(3A)
(4A)
4164
(1C)
(1B)
81256
(2C)
(2B)
J1
J2
J3
C11
C5
C6
C13
C12
C18
C20
C1
C2
C3
C4
C14
C16
C17
C15
R15
20K
0.1u
47u
16v
33*14
EQUITY Ⅱ+/PC AX2
ADR-RM3 BOARD Unit No.:Y162204 10000(B-3)



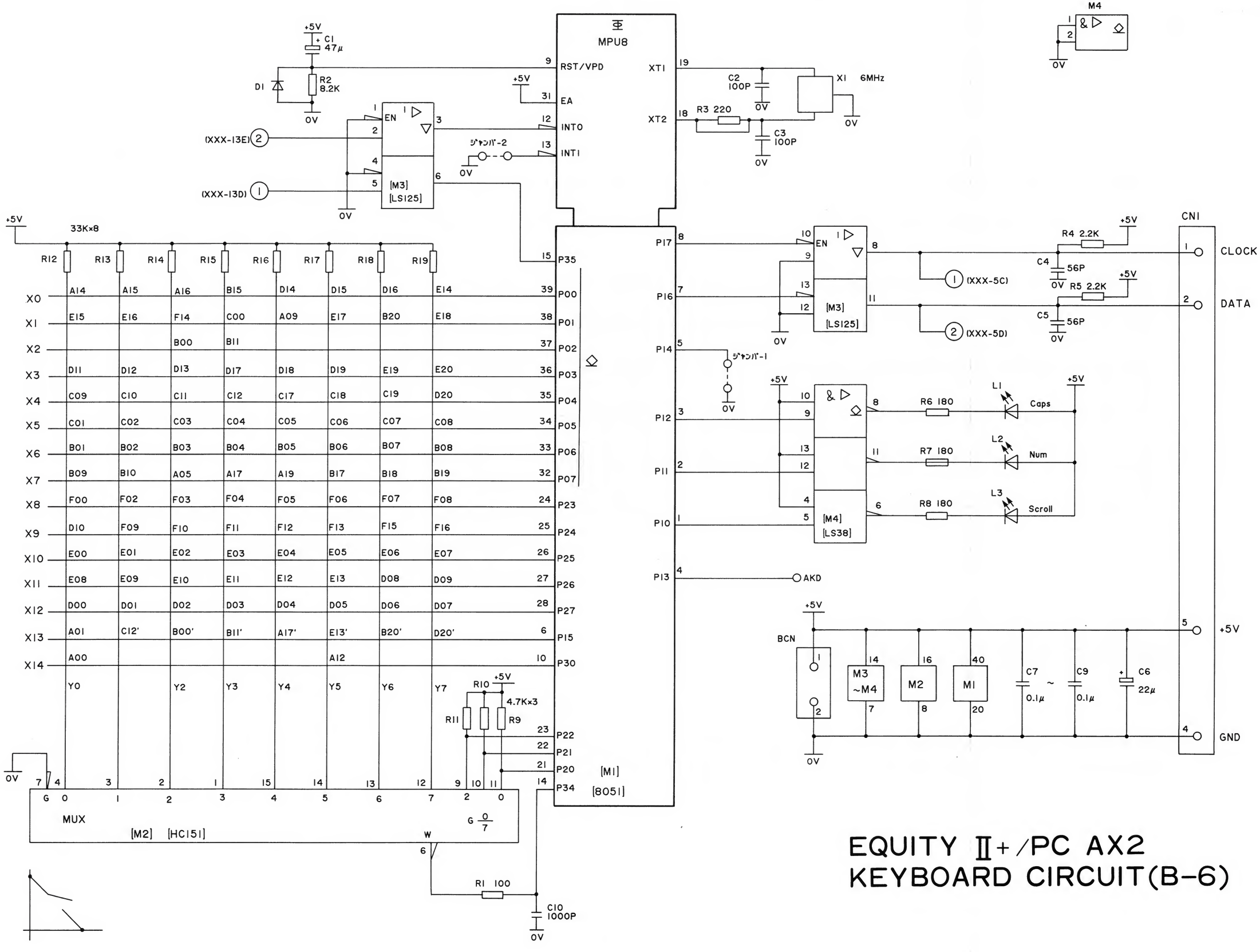
VERSION	DATE	DESIGN	CHECK	DESCRIPTION	TITLE	PAGE
A	'87. 4.14	Y.NAKAOKA			ADR-RM3S	1/1
					MODEL: ANDROMEDA	VERSION: A
					SCHEMATIC NUMBER	
					APD Hirooka, EPSON America Inc.	

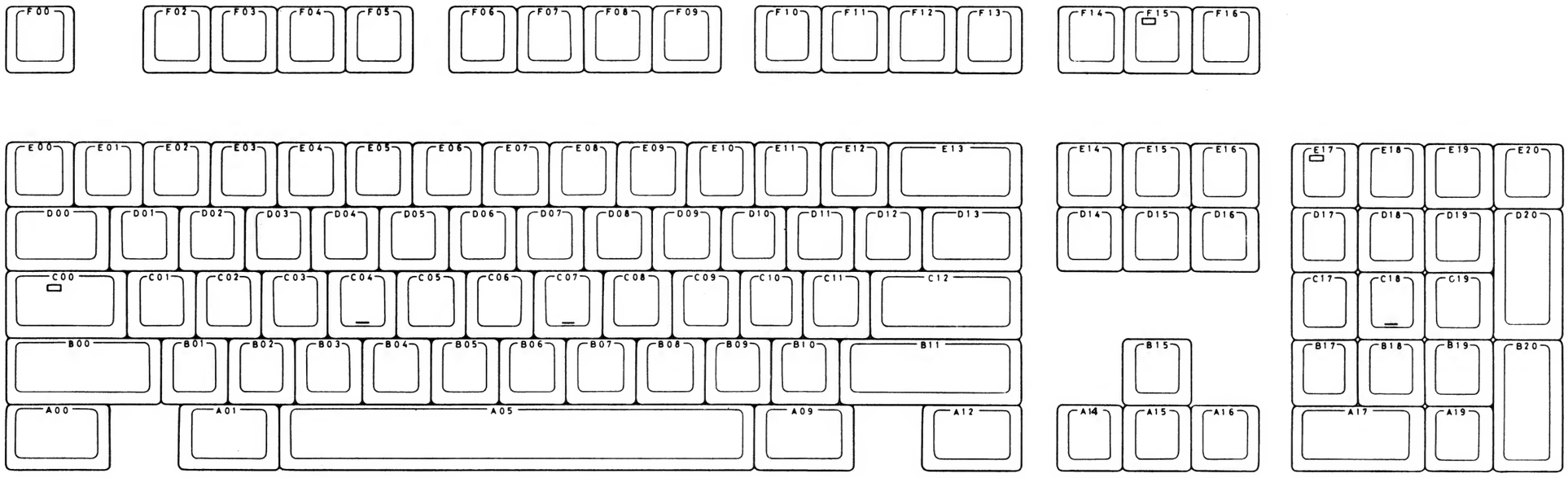
EQUITY Ⅱ+/PC AX2
ADR-RM3S BOARD Unit No,:Y16220500000(B-4)



EQUITY Ⅱ+/PC AX2 ADR-PS UNIT(B-5)

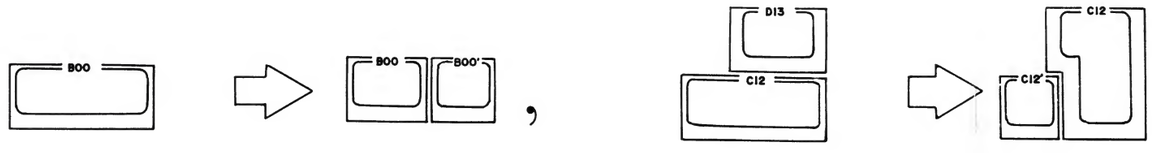
EQUITY Ⅱ+/PC AX2
KEYBOARD CIRCUIT(B-6)

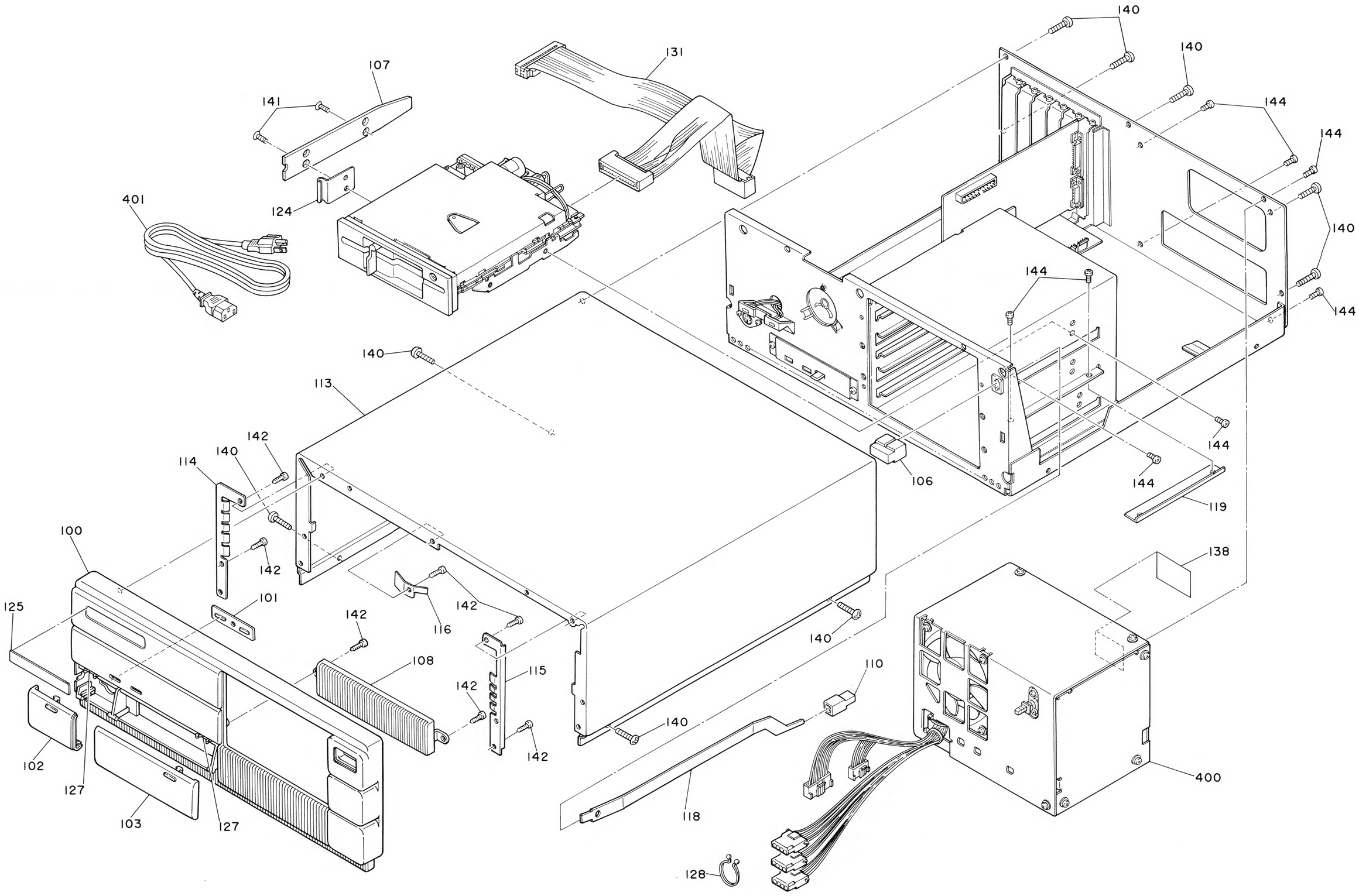




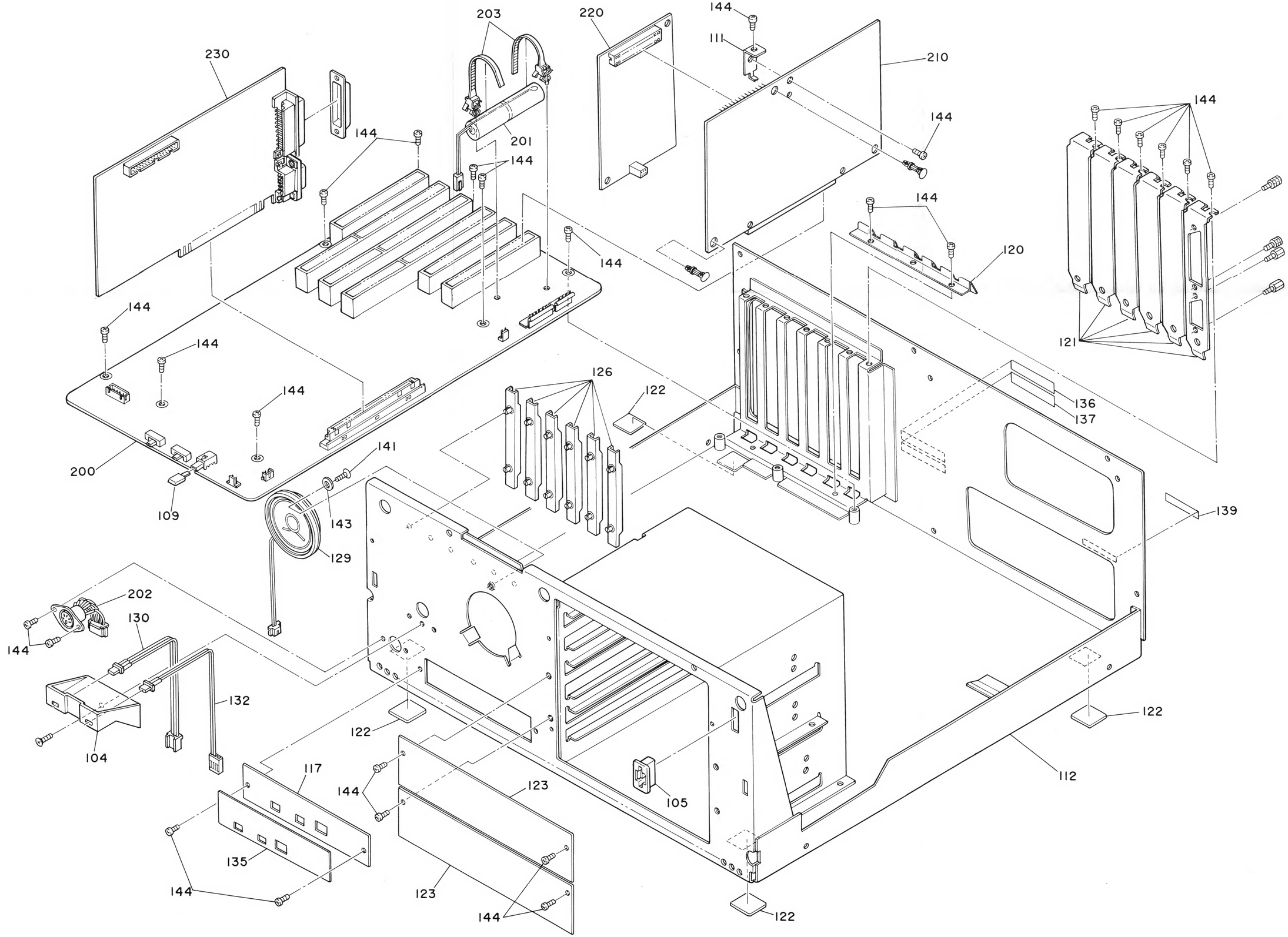
101-Key board Layout

(NOTE: 102-Key board)





EQUITY II+ /EPSON PC AX2 EXPLODED DIAGRAM(1/2)(B-7)



EQUITY Ⅱ+ /EPSON PC AX2 EXPLODED DIAGRAM(2/2)(B-8)

EPSON OVERSEAS MARKETING LOCATIONS

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Dorland House, 388 High Road,
Wembley, Middlesex, HA9 6UH, U.K.
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Telex: 8814169

EPSON – SEGI S.p.A.
Via Timavo, 12 20124 Milano
Phone: 02 – 6709136
Telex: 315132 SEGI I

EPSON AUSTRALIA PTY. LTD.
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Forest, NSW 2086, Australia
Phone: 02 – 452 – 5222
Telex: 75052

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Road, Wanchai, Hong Kong
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Telex: 65542 EPSON HX

EPSON DEUTSCHLAND GmbH
Zulpicher Strasse 6 4000 Dusseldorf
11 F.R. Germany
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Telex: 8584786

EPSON FRANCE S.A.
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Roche, 92230 Genneviliers
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Telex: RS 39536 EPSONS

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SEIKO EPSON CORPORATION
80 Hirooka Shiojiri – shi, Nagano
399 – 07, Japan
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Telex: 3342 – 214

EPSON

Printed in Japan 87.09 – 1.5

PARTS PRICE LIST

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SERVICE DIVISION

EPSON

EPSON AMERICA, INC.
23155 KASHIWA COURT, TORRANCE, CALIFORNIA 90505
PHONE (213) 534-0360 TELEX 182412

EQUITY II+

PARTS PRICE LIST

July 23, 1987

(CONTENTS SUBJECT TO CHANGE WITHOUT NOTICE)

M-PL-EQII+

SECTION: CASE COMPONENTS

MODEL: EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
100	Y162010051	FRONT COVER (162-1100)	1	22.50	
101	Y162011051	LED LENS (162-1110)	1	1.70	
102	Y162012051	LID A (162-1120)	1	2.80	
103	Y162013051	LID B (162-1130)	1	3.68	
104	Y162014051	LED SUPPORT (162-1140)	1	1.50	
105	Y162015051	PUSH ROD GUIDE (162-1150)	1	0.90	
106	Y162016051	POWER SWITCH BUTTON (162-1160)	1	2.30	
107	Y162017051	D/D RAIL (162-1170)	1	3.44	
108	Y162018051	STORAGE SLOT COVER (162-1180)	1	4.16	
109	Y147038001	RESET BUTTON (147-2210)	1	0.25	
110	Y162027051	ROD CONNECTOR P (162-1270)	1	1.00	
111	Y162019051	MEMORY BOARD SUPPORT (162-1190)	1	1.30	
112	Y162020051	LOWER CASE (162-1200)	1	154.50	
113	Y162021051	UPPER COVER (162-1210)	1	65.55	
114	Y162022051	EARTH PLATE A (162-1220)	1	3.10	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
115	Y162023051	FRONT EARTH PLATE B (162-1230)	1	3.10	
116	Y162024051	FRONT EARTH PLATE C (162-1240)	1	1.10	
117	Y162025051	FRONT PANEL 01 (162-1250)	1	2.40	
118	Y162026051	PUSH ROD (162-1260)	1	3.30	
119	Y162028051	D/D SHELF (162-1280)	1	3.10	
120	Y162031051	REAR EARTH PLATE A (162-1310)	1	3.50	
121	Y144518000	OP. CONNECTOR GUIDE A	5	1.80	
122	Y162032051	FOOT (162-1320)	4	2.90	
123	Y162033051	STORAGE SLOT PANEL (162-1330)	2	3.20	
124	Y162034051	D/D EARTH (162-1340)	1	1.30	
125	Y162035051	LOGO PLATE 01 (162-1350)	1	3.36	
126	X550000060	GUIDE RAIL (GR-80S)	6	2.80	
127	X510120000	PUSH LOCK (2A16)	2	2.10	
128	X510060100	PURSE LOCK (SINGLE TYPE)	1	0.25	

SECTION: CASE COMPONENTS

MODEL: EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
129	Y162300300	CABLE SET #5CK	1	8.24	
130	Y162300200	CABLE SET #5CW	1	8.48	
131	Y144314000	CABLE SET #5CB	1	50.10	
132	Y162300100	CABLE SET #5CU	1	13.12	
133	Y162300400	CABLE SET #5DC	1	16.50	
134	Y162300500	CABLE SET #5DD	1	39.60	
135	Y162036051	FRONT PANEL LABEL (162-1360)	1	3.90	
136	Y911037801	UL CSA LABEL 08 (911-1300)	1	0.70	
137	Y901026001	GS-TUV LABEL (901-1070)	1	0.40	
138	Y147039001	VOLTAGE SWITCH LABEL 01	1	0.90	FOR 100-120V
139	Y162041051	AC OUTLET LABEL	1	0.40	
140	Y911041051	FIXING SCREW 3 (911-1330)	9	0.25	
141	Y126019051	SCREW (M3.505x8)	4	0.90	
142	B018201811	C.T.B.SCREW (M3x10)	7	0.10	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
143	B090200911	PLAIN WASHER (4.3x0.8x9)	1	0.10	
144	Y144038003	SCREW (NI) (M3.5X4)	34	0.80	

SECTION: ANDRO PCB UNIT COMPONENTS

MODEL: EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
200	Y162201100	ANDRO PCB UNIT WITHOUT CPU	1	750.00	
201	Y126510000	LITHIUM BATTERY CR17335SE-T (2CL102)	1	52.55	
202	Y126308000	CABLE SET #5BZ (K.B. CONNECTOR)	1	12.96	
203	X510060030	WIRE BAND (SG-130)	2	0.40	
F1	X502013020	FUSE (120V 5000MA)	1	1.80	
1B	X440147580	SSI (IC) T4758	1	55.60	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
210	Y162204100	EQ2+ ADR-RM3 PCB UNIT	1	278.38	
3B	Y162802000	P-ROM (27128-ADR-A1)	1	52.80	
3B,4B	X630112830	IC SOCKET (28 PIN)	2	2.10	
4B	Y162803000	P-ROM (27128-ADR-B1)	1	52.80	

SECTION: EQ2+ ADR-RM3S PCB UNIT COMPONENTS **MODEL:** EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
220	Y162205000	EQ2+ ADR-RM3S PCB UNIT	1	274.72	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
230	Y162203100	EQ2+ SPF2 PCB UNIT	1	285.71	
231	Y126007052	OP. BOARD FIXING PLATE C	1	3.90	

SECTION: WHDC CIRCUIT BOARD UNIT COMPONENTS

MODEL: EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
240	Y127203100	WHDC CIRCUIT BOARD UNIT	1	461.54	
241	Y126022052	OP.BOARD FIXING PLATE D (126-1230 NI)	1	5.28	
4H	X400310154	LSI (BUF.MANAGE CONT.PROCESS)	1	64.20	
4H	X630114030	IC SOCKET (40 PIN)	1	2.10	
6F	X400311001	LSI (BUFFER MANAGER AND CONTROLLER)	1	89.80	
6F	X630118400	IC SOCKET (84 PIN LCS)	1	23.10	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
400	Y162501000	POWER SUPPLY UNIT ADRPS	1	337.62	
401	Y901300100	POWER CABLE (120V UL-CSA)	1	23.88	FOR U.S.A.

SECTION: FLOPPY DISK DRIVES

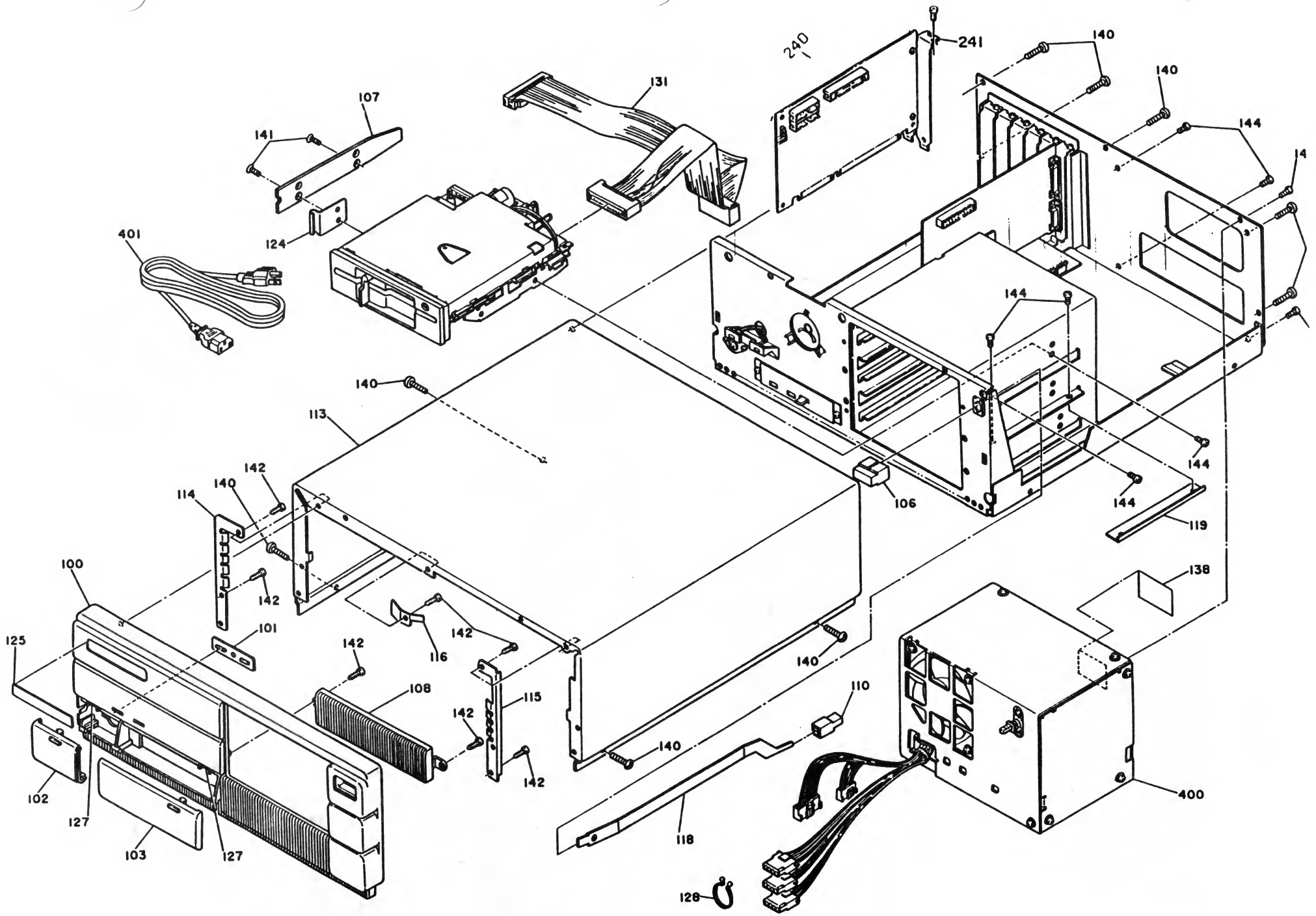
MODEL: EQUITY II+

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
	A112A-AA	3.5" 720KB FDD	1	169.00	
	Q213A-AA	360KB FDD	1	199.00	

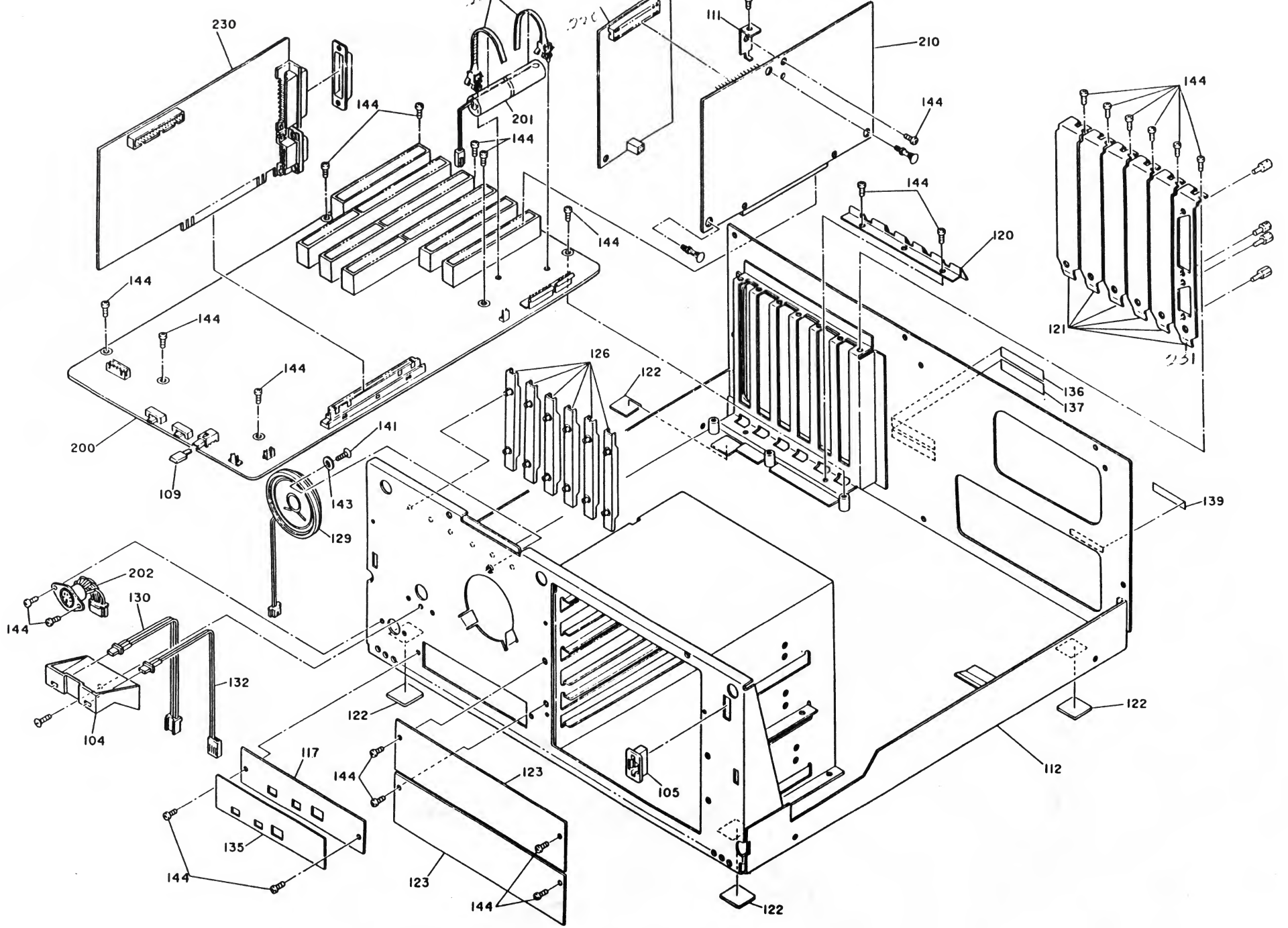
SECTION: PACKING MATERIALS

MODEL: EQUITY II+

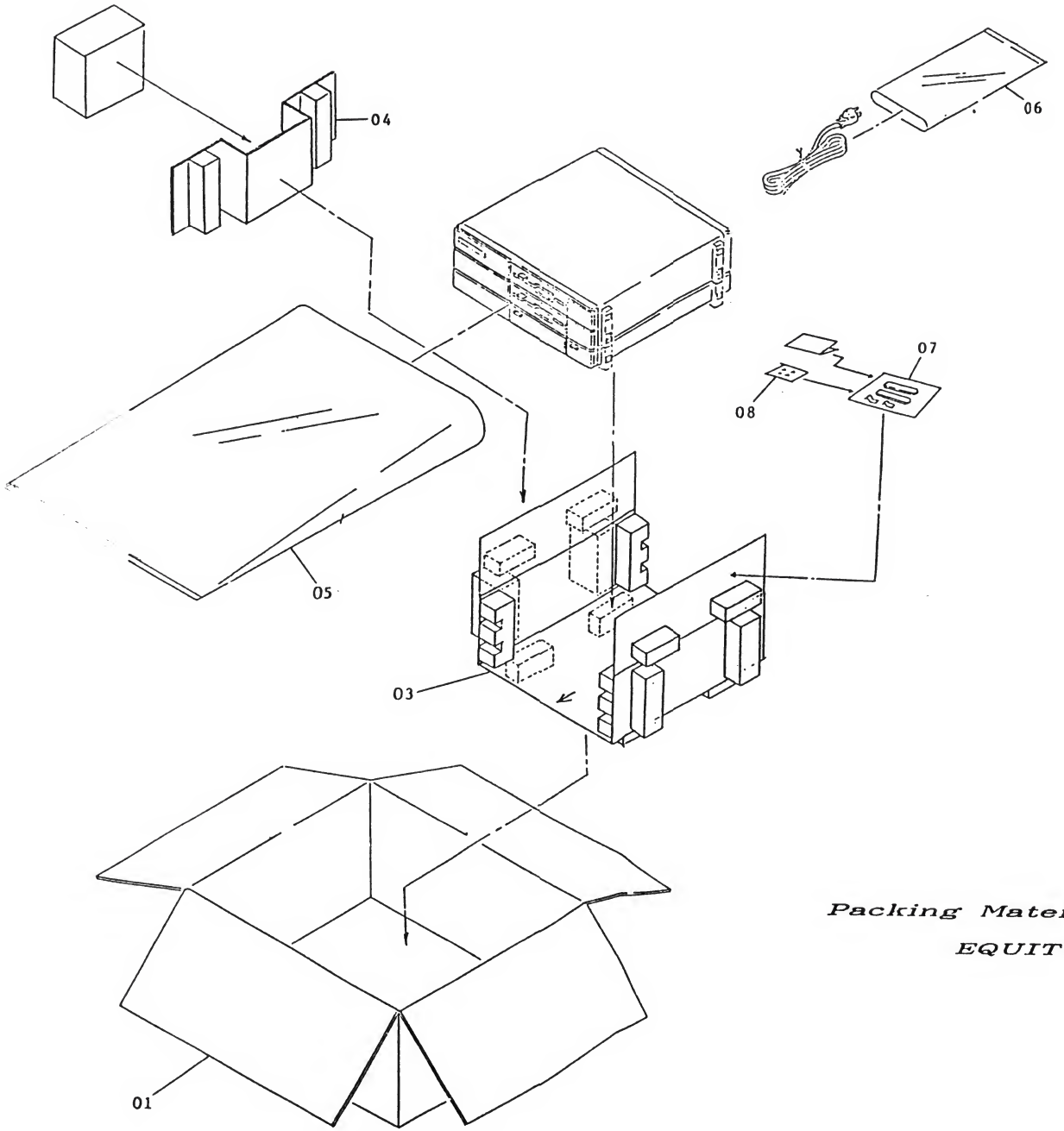
REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
01	Y162931001	INDIVIDUAL CARTON BOX - EQII+	1	11.13	
03	Y162933001	PACKING CUSHION - EQII+	1	9.11	
04	Y162933002	PAD FOR MANUAL - EQII+	1	2.53	
05	Y132932001	PLASTIC PROTECTIVE BAG - EQII+	1	0.35	
06	Y422932003	PLASTIC BAG - EQII+	1	0.25	
07	X680120010	PLASTIC BAG (200x140x0.04T) - EQII+	1	0.25	
08	X680119010	PLASTIC BAG - EQII+	1	0.25	



Exploded Diagram For EQUITY II+



Exploded Diagram For EQUITY II+



Packing Material For
EQUITY II+,

BULLETINS

EPSON

SERVICE DIVISION

EPSON
EQUITY II+
CERTIFICATION LISTINGS

Produced by Epson Systems Product Assurance

Advanced Products Development

23 September, 1987

As a service to our customers, Epson America Inc. ("EPSON") has implemented an ongoing program to test software and hardware products for use with the Equity series of personal computers.

The following information includes products that have been tested by Epson Japan - APD, Epson America - APD Product Assurance and/or the product vendor for use with the Epson Equity II+ personal computer. This list does not include every product that operates with the Epson Equity II+ computer. Epson will update this list from time to time. The list is subject to change without notice.

Unless otherwise noted, all tests were conducted with the latest release of the Equity MS-DOS operating system software and ROM BIOS.

The information provided does not constitute a guarantee or endorsement of any particular product for any specific use or application. Some of the products on the list may have software or hardware requirements which are not met by the Epson Equity II+ personal computer. Therefore, while EPSON believes the information supplied is accurate, EPSON does not assume any responsibility for use of any of the products on the attached list.

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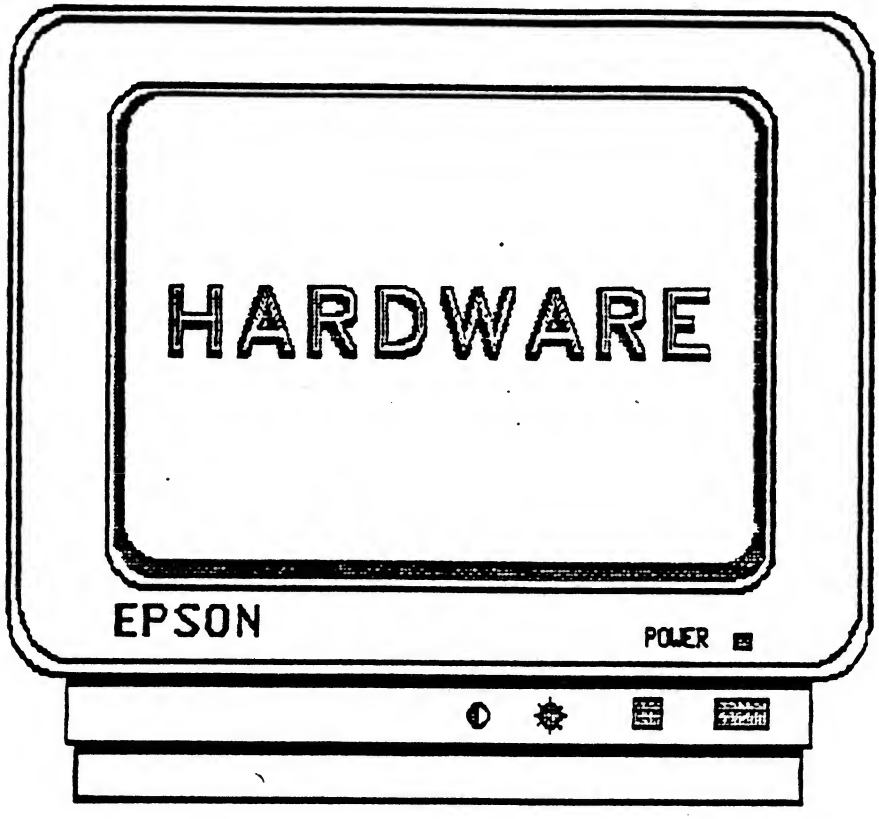
Since the Equity II+ is capable of operating at 8 and 10 MHz, the listing reflects these two speeds. In general, if an entry has been tested at both speeds, it will be indicated in the listings.

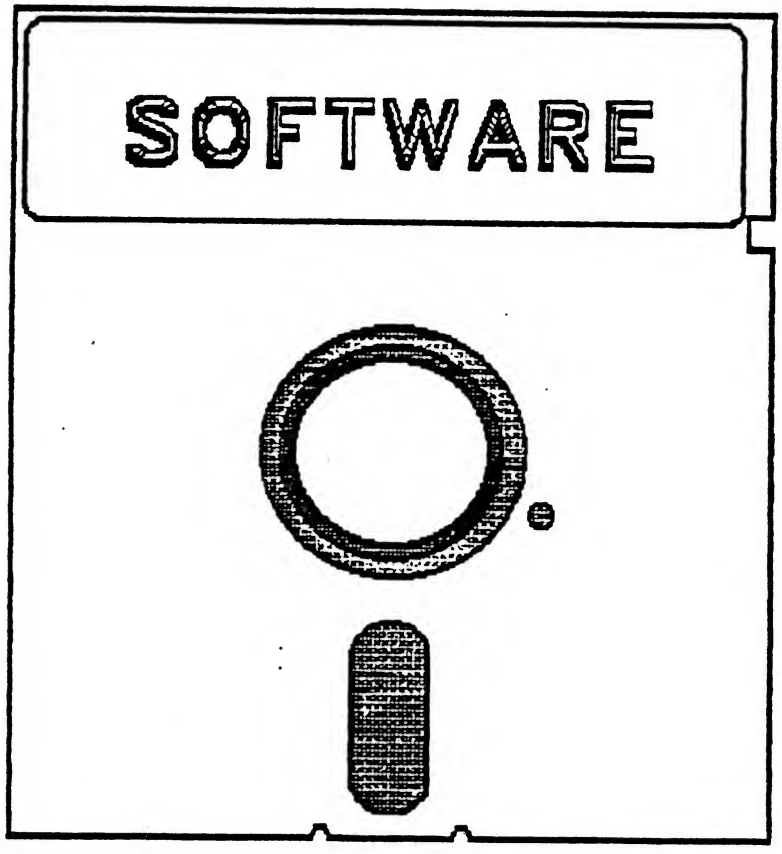
If a product has been tested and passed at 10 MHz, it is assumed that it will also operate as expected at 8 MHz. In this case, only the 10 MHz speed would be marked in the listings.

If a product in the listings is marked at only 8 MHz, this indicates that it may not function properly at the higher speed. This is most likely to occur with networking, terminal emulation, tape backup systems or memory expansion boards and some forms of software copy protection.


HARDWARE
EPSON
POWER

EQUITY. II+ TESTED HARDWARE LISTING

CATEGORY	PRODUCT	MODEL	VENDOR	CPU SPEED 8	CPU SPEED 10	NOTES
EXPANDED MEMORY	ABOVEBOARD	AT	INTEL CORP.		X	
FLOPPY DISK DRIVES	1.2MB - 5.25"	MD-5501	CANON U.S.A., INC.		X	
	360KB - 5.25"	MD-5201	CANON U.S.A., INC.		X	
	720KB - 3.5"	SMD-400	EPSON AMERICA, INC.		X	
FIXED DISK CONTROLLERS	SPF CONTROLLER BOARD		EPSON AMERICA, INC.	X	X	
FIXED DISK DRIVES	20MB - HH 3.5"	HMD-720	EPSON AMERICA, INC.		X	
	40MB - FH	6053	MINISCRIBE CORP.		X	
	40MB - HH	94205-51	CONTROL DATA CORP.		X	
	40MB - HH	5146H	NEC		X	
INPUT DEVICES	KEYBOARD - 101 KEY	AT	IBM	X	X	
	MOUSE - BUS	---	EPSON AMERICA, INC.	X	X	
	MOUSE - SERIAL	---	MOUSE SYSTEMS CORP.		X	
MISCELLANEOUS	MATH COPROCESSOR	80287 (8MHz)	INTEL CORP.	X	X	
	MICROBUFFER - 64KB	---	PRACTICAL PERIPHERALS, INC.	X	X	
MODEMS	COURIER 2400	EXTERNAL	US ROBOTICS, INC.		X	
	LINK 1200	EXTERNAL	EPSON AMERICA, INC.		X	
	LINK 1200 PC	INTERNAL	EPSON AMERICA, INC.		X	
	SMARTMODEM 1200	EXTERNAL	HAYES MICROCOMP. PROD. INC.	X	X	
	SMARTMODEM 1200B	INTERNAL	HAYES MICROCOMP. PROD. INC.	X	X	
MONITORS	RGB - 13"	MCM-4035N-E	EPSON AMERICA, INC.		X	
	EGA - 13"	MCH-4095E	EPSON AMERICA, INC.		X	
	EGA	---	IBM		X	
	MONOCHROME	---	IBM		X	
	MONONCHROME- GREEN 12"	MBM-2095-E	EPSON AMERICA, INC.		X	
PERIPHERAL PORTS	ASYNCH CARD		IBM	X	X	
VIDEO BOARDS	AUTOSWITCH EGA	02-10	PARADISE SYSTEMS, INC.		X	
	COLOR GRAPHICS ADAPTER	Q505A-AA	EPSON AMERICA, INC.	X	X	
	COLOR GRAPHICS ADAPTER	---	IBM		X	
	MONO DISPLAY/PRINTER ADAPTER	---	IBM	X	X	
	MONOCHROME ADAPTER	Q508A-AA	EPSON AMERICA, INC.	X	X	
	MULTIMODE GRAPHICS ADAPTER	Q205A-AA	EPSON AMERICA, INC.		X	


SOFTWARE

EQUITY II+ TESTED SOFTWARE LISTING

CATEGORY	PRODUCT	VERSION	VENDOR	CPU SPEED 8	CPU SPEED 10	NOTES
COMMUNICATIONS	CROSSTALK XVI	3.5	MICROSTUF, INC.	X	X	
	CROSSTALK XVI	3.6	MICROSTUF, INC.		X	
	LAPLINK	2.04	TRAVELLING SOFTWARE, INC.		X	
	PFS:ACCESS	C.04	SOFTWARE PUBLISHING CORP.	X	X	
	PROCOMM	2.4.2	PIL SOFTWARE SYSTEMS		X	
DATABASE	dBASE III+	1.1	ASHTON-TATE		X	
	dFLOW	3.15B	WALLSOFT SYSTEMS, INC.		X	
	RAPIDFILE	1.0	ASHTON-TATE		X	
	R:BASE 5000	1.01	MICRORIM	X	X	
DESKTOP MANAGER	TOPVIEW	1.0	IBM	X		
	WINDOWS	1.0	MICROSOFT CORP.		X	
DESKTOP PUBLISHING	PAGEMAKER	1.0a	ALDUS CORP.		X	
	PFS:FIRST PUBLISHER	1.00	SOFTWARE PUBLISHING CORP.	X		
ENTERTAINMENT	F-15 STRIKE EAGLE	1985	MICROPROSE	X		
	JET	1985	SUBLOGIC CORP.	X	X	
	LODE RUNNER	1983	BRODERBUND SOFTWARE	X		
	SARGON III	1984	HAYDEN SOFTWARE, INC.	X		
GRAPHICS	MICROSOFT PAINTBRUSH	1.0	MICROSOFT CORP.		X	
	MICROSOFT SHOW PARTNER	2.0	MICROSOFT CORP.		X	
INTEGRATED	FRAMEWORK II	1.1	ASHTON-TATE		X	
	PFS:FIRST CHOICE	1.0	SOFTWARE PUBLISHING CORP.		X	
LANGUAGES	GW-BASIC	3.2	EPSON AMERICA, INC.	X	X	
OPERATING SYSTEMS	MS-DOS 3.2	2.0	EPSON AMERICA, INC.	X	X	
	XENIX SYSTEM V (286)	R.2.1	SANTA CRUZ OPERATION	X		
SPELLING CHECKERS AND THESAURUS'S	TURBO LIGHTNING	4.40	BORLAND INTERNATIONAL, INC.		X	

EQUITY II+ TESTED SOFTWARE LISTING

CATEGORY	PRODUCT	VERSION	VENDOR	CPU SPEED 8	CPU SPEED 10	NOTES
SPREADSHEET	LOTUS 1-2-3	2	LOTUS DEVELOPMENT CORP.	X	X	
	PFS:PROFESSIONAL PLAN	1.0	SOFTWARE PUBLISHING CORP.		X	
	SUPERCALC 3	2.1	COMPUTER ASSOCIATES		X	
	SUPERCALC 4	1.0	COMPUTER ASSOCIATES		X	
UTILITY	NORTON COMMANDER	1.0	PETER NORTON COMPUTING		X	
	NORTON UTILITIES	3.0	PETER NORTON COMPUTING	X	X	
	NORTON UTILITIES	4.0	PETER NORTON COMPUTING	X	X	
	NORTON ADVANCED UTILITIES	4.0	PETER NORTON COMPUTING	X	X	
	SIDEKICK	1.56B	BORLAND INTERNATIONAL, INC.		X	
	SPEEDSTOR	4.02A	STORAGE DIMENSIONS		X	
WORD PROCESSING	PFS:PROFESSIONAL WRITE	1.0	SOFTWARE PUBLISHING CORP.		X	
	WORDPERFECT	4.1	WORDPERFECT	X	X	
	WORDSTAR	3.31P	MICROPRO INTERNATIONAL CORP.	X	X	
	WORDSTAR PROFESSIONAL	4	MICROPRO INTERNATIONAL CORP.		X	

EPSON
EPSON AMERICA, INC.
Computer Products Division

MARKETING INFORMATION BULLETIN

DATE: 12/18/87 NO: SM0056

FROM: Jackie Lujan-Medina / Product Management-Systems

SUBJECT: AT-TYPE HARD DISK DRIVE CONTROLLER

****

This is to announce the availability of the AT-TYPE HARD DISK DRIVE CONTROLLER for the EQUITY II+ and EQUITY III+. This product will be available the week of 12/21/87.

As you are aware, the single floppy version of the EQUITY II+ and III+ no longer includes a hard disk drive controller. This product serves as an add-on option when a user decides to upgrade the system to include a 40MB hard disk drive. This controller is the same as the controller that comes standard with the EQUITY II+ and EQUITY III+ hard disk version.

It can also be used with any hard disk drive that has been tested by Epson. Attached, please find listings of hard disk drives that have been tested for both the EQUITY II+ and EQUITY III+. These listings are referenced in the EQUITY II+/III+ Compatibility Guide.

Please contact me if you should have any questions.

EPSON AMERICA, INC.
Vice President, Sales
2780 Lomita Blvd
Torrance, CA 90505
Building 4, MS 4-6
213/539-9140 x4220

December 18, 1987

MEMORANDUM TO: Zone Managers, District Managers, Sales Trainers and Sales Representatives

SUBJECT: NEW PRODUCT ANNOUNCEMENT:

AT-TYPE HARD DISK DRIVE CONTROLLER

The purpose of this memo is announce the AT-Type Hard Disk Drive Controller, a new option product for the EQUITY II+ and EQUITY III+. This product is available for immediate shipment.

As you are aware, the single floppy version of the EQUITY II+ and III+ no longer includes a hard disk drive controller. This product serves as an add-on option when a user decides to upgrade the system to include a 40MB hard disk drive. It can also be used with any hard disk drive that has been tested by Epson and is listed in the EQUITY II+ /III+ Compatibility Guide. This controller is the same as the controller that comes standard with the EQUITY II+ and EQUITY III+ hard disk version.

Please see attached Marketing Information Bulletin for additional product information. Pricing information is detailed in the January 1, 1988 National Price Sheet.

C. A. Jenks

Copies to:

Torrance Marketing & Sales Staff
G. Kunde
E. Ide
B. Page
J. Lang
D. Bulot
C. Hodowski
L. Holsopple
D. Hammer
L. Babin
A. Pound
J. Cirillo
C. Turlington

EQUITY II+ TESTED HARDWARE LISTING

CATEGORY	PRODUCT	MODEL	VENDOR	CPU SPEED 8	CPU SPEED 10	NOTES
EXPANDED MEMORY	ABOVEBOARD	AT	INTEL CORP.		X	
FLOPPY DISK DRIVES	1.2MB - 5.25"	MD-5501	CANON U.S.A., INC.		X	
	360KB - 5.25"	MD-5201	CANON U.S.A., INC.		X	
	720KB - 3.5"	SMD-400	EPSON AMERICA, INC.		X	
FIXED DISK CONTROLLERS	SPF CONTROLLER BOARD		EPSON AMERICA, INC.	X	X	
FIXED DISK DRIVES	20MB - HH 3.5"	HMD-720	EPSON AMERICA, INC.		X	
	40MB - FH	8053	MINISCRIBE CORP.		X	
	40MB - HH	94205-51	CONTROL DATA CORP.		X	
	40MB - HH	5146H	NEC		X	
INPUT DEVICES	KEYBOARD - 101 KEY	AT	IBM	X	X	
	MOUSE - BUS	---	EPSON AMERICA, INC.	X	X	
	MOUSE - SERIAL	---	MOUSE SYSTEMS CORP.		X	
MISCELLANEOUS	MATH COPROCESSOR	80287 (8MHz)	INTEL CORP.	X	X	
	MICROBUFFER - 64KB	---	PRACTICAL PERIPHERALS, INC.	X	X	
MODEMS	COURIER 2400	EXTERNAL	US ROBOTICS, INC.		X	
	LINK 1200	EXTERNAL	EPSON AMERICA, INC.		X	
	LINK 1200 PC	INTERNAL	EPSON AMERICA, INC.		X	
	SMARTMODEM 1200	EXTERNAL	HAYES MICROCOMP. PROD. INC.	X	X	
	SMARTMODEM 1200B	INTERNAL	HAYES MICROCOMP. PROD. INC.	X	X	
MONITORS	RGB - 13"	MCM-4033N-E	EPSON AMERICA, INC.		X	
	EGA - 13"	MCM-4095E	EPSON AMERICA, INC.		X	
	EGA	---	IBM		X	
	MONOCHROME	---	IBM		X	
	MONOCHROME- GREEN 12"	MBM-2095-E	EPSON AMERICA, INC.		X	
PERIPHERAL PORTS	ASYNCH CARD		IBM	X	X	
VIDEO BOARDS	AUTOSWITCH EGA	02-10	PARADISE SYSTEMS, INC.		X	
	COLOR GRAPHICS ADAPTER	G505A-AA	EPSON AMERICA, INC.	X	X	
	COLOR GRAPHICS ADAPTER	---	IBM		X	
	MONO DISPLAY/PRINTER ADAPTER	---	IBM	X	X	
	MONOCHROME ADAPTER	G508A-AA	EPSON AMERICA, INC.	X	X	
	MULTIMODE GRAPHICS ADAPTER	G205A-AA	EPSON AMERICA, INC.		X	

(12 MHz)

EQUITY III+/e TESTED HARDWARE LISTING

CATEGORY	PRODUCT	MODEL	VENDOR	CPU SPEED 6	8	12	NOTES
EXPANDED MEMORY BOARDS	ABOVE BOARD AT	---	INTEL CORP.			X	
FDD CONTROLLERS	SPFG CONTROLLER	---	EPSON AMERICA, INC.			X	
FLOPPY DISK DRIVES	1.2MB - 5.25"	MD-5501	CANON U.S.A., INC.			X	
	1.2MB - 5.25"	FD-1155C	NEC			X	
	360KB - 5.25"	MD-5201	CANON U.S.A., INC.			X	
	720KB - 3.5"	SMD-400	EPSON AMERICA, INC.			X	
FIXED DISK CONTROLLERS	FXD CONTROLLER	---	EPSON AMERICA, INC.			X	
FIXED DISK DRIVES	20MB - 3.5"	MMD-720	EPSON AMERICA, INC.			X	
	40MB - FH	6053	MINISCRIBE CORP.			X	
	40MB - HH	94205-51	CONTROL DATA CORP.			X	
	60MB - HH	DS127H	NEC			X	
	30MB - HH	DS147H	NEC			X	
INPUT DEVICES	JOYSTICK	---	KRAFT SYSTEMS CO.			X	
	KOALAPAD	---	KOALA TECHNOLOGIES CORP.			X	
	MICROSOFT MOUSE - BUS	5.03	MICROSOFT CORP.			X	
	MICROSOFT MOUSE - SERIAL	---	MICROSOFT CORP.			X	
	MOUSE - BUS	---	EPSON AMERICA, INC.			X	
LOCAL AREA NETWORKS	PC NETWORK	---	IBM		X		
MISCELLANEOUS	80287 COPROCESSOR	8 MHz	INTEL CORP.			X	
	COPY II PC BOARD		CENTRAL POINT SOFTWARE		X		
MODEMS	LINK 1200	EXTERNAL	EPSON AMERICA, INC.			X	
	LINK 1200 PC	INTERNAL	EPSON AMERICA, INC.			X	
	SMARTMODEM 1200	EXTERNAL	HAYES MICROCOMP. PROD., INC.			X	
	SMARTMODEM 1200B	INTERNAL	HAYES MICROCOMP. PROD., INC.			X	
MONITORS	CGA - 13"	MCM-4033N-E	EPSON AMERICA, INC.			X	
	CGA	---	IBM			X	
	EGA	MCM-4095E	EPSON AMERICA INC.			X	
	EGA	---	IBM			X	

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/2/87 NUMBER: S-0001B

SUBJECT: EQUITY SERIES FDD/HDD COMPATIBILITY MATRIX

This document provides updated compatibility information on floppy disk drives, hard disk drives and hard disk controllers which have been supplied or are currently being supplied with the Equity series computers from Epson America, Inc.

The Equity I+, Equity II+ and Equity III+ computers have been included in this matrix.

Also included is information on which low level hard disk format procedures should be used with the various versions of hard disk controller boards.

Please refer to the Equity I, II, III IBM-PC COMPATIBLE HARDWARE/ SOFTWARE DIRECTORY supplied by Epson America's Marketing Department for information regarding third party floppy disk and hard drive compatibility.

EQUITY SERIES FLOPPY DISK DRIVE COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
360KB 5.25" FDD	I	I+	II	II+	III	III+	
MDD-531-51 (CANON)	X						
MD-5201-55 (CANON)	X						C
SD-525-501 (EPSON)	X						
MDD-531-31 (EPSON)			X		X		A,J
MD-5201-57 (CANON)		X	X	X	X	X	D,E
MD-5201-58 (CANON)		X	X	X	X	X	D,E,I
SD-521-506 (EPSON)		X	X	X	X	X	B
1.2MB 5.25" FDD	I	I+	II	II+	III	III+	
SD-580 (EPSON)					X		G
SD-581L-501 (EPSON)			X				B,F,G,H
JU-595-10 PANASONIC					X		
MD-5501-61 (CANON)				X	X	X	
FD1155C/FD1157C NEC				X	X	X	
720KB 3.5" FDD	I	I+	II	II+	III	III+	
SMD-489M (EPSON)		X	X	X	X	X	

COMMENT CODE EXPLANATIONS:

A. Requires insulating sheet when installed in lower position in Equity II. See TIB Equity II-006.
B. Jumper block SS1 - Position DS0 for drive A, DS1 for drive B
C. Equity I must have ROM BIOS version 2.21(MSA-B4) and MS-DOS 2.11 Release 1.04 or higher to use this drive.
D. Must set drive select jumpers on FDD logic board for A (position S1) or B (position S2).
E. It is not necessary to remove the terminating resistor pack.
F. Handle drive with care - possibility of short circuit between screw head on frame and FDD logic board (could damage FDD)!
G. Terminator must be removed when used as 2nd floppy drive unit.
H. See Product Support Bulletin S-0020 for set-up information.
I. Same as MD-5201-57 except comes configured as 2nd drive.
J. Jumper block JJ1 - Position S1 for drive A, S2 for drive B.

EQUITY SERIES HARD DISK DRIVE COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
20MB HARD DISK DRIVES	I	I+	II	II+	III	III+	
DK-505-2 (HITACHI)	X						C
HD-860-501/502/503	X	X	X				
HMD-720-802 EPSON	X	X	X		X		D
HMD-720-803 EPSON				X	X	X	
HD-860-504/505 EPSON	X	X	X	X	X	X	A, B
HD-860-506 EPSON	X	X	X	X	X	X	B
40MB HARD DISK DRIVES	I	I+	II	II+	III	III+	
D5146 (NEC)				X	X	X	
6053 (MINISCRIBE)				X		X	
94205-51 (CDC)				X		X	

COMMENT CODE EXPLANATIONS:

A. Comes with black front bezel.
B. When used with Equity III use format procedure #2 on page 5.
C. Follow format procedure #2 on page 5. The NCL Hard Disk Controller Board (NDC5027-49) and DK-505-2 HDD must be used together.
D. For Equity III - Only use HMD-720 hard drives NOT stamped with: "Do not use with Equity III".

EQUITY SERIES HARD DISK CONTROLLER COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
HARD DISK CONTROLLER	I	I+	II	II+	III	III+	
WD1002S-WX2C027 ROM 62-000062-010	X						B,E
WD1002S-WX2C027 ROM 62-000062-010-1	X	X	X				B
WD1002A-WX1E027 ROM 62-000062-010-1 or 62-000062-13	X	X	X				B,C,D
NCL NDC5207-49	X						A
WD1002-WAH ROM 62-001020-10 AND 62-001027-11					X		
EPSON WHDC BOARD P/N Y127203000 ROM VERSION WD1015PL-27 or -27B 62-002008-011 or -061				X		X	F,G

CODE EXPLANATIONS:

A. Follow format procedure #2. NCL Hard Disk Controller Board (NDC5027-49) and DK-505-2 HDD must be used together

B. Follow format procedure indicated on PSB # S-0005.

C. Short version Western Digital HDC board. Released late 1986.

D. ROM BIOS 62-000062-010-1 and 62-000062-13 are equivalent. Either ROM may be found on this board.

E. This version HDC ROM BIOS with WD-1015-24 firmware CPU will not allow auto-boot from hard disk. WD-1015-14 firmware CPU will work.

F. ROM BIOS # WD1015PL-27 is equivalent to 62-002008-011 these ROMs have been updated to # WD1015PL-27B or 62-002008-061 which are also equivalent to each other.

G. HDC ROM BIOS must be revision "B" to work with XENIX software.

HARD DISK FORMATTING INFORMATION

```
*****IMPORTANT**************IMPORTANT******************IMPORTANT******
*                                                                     *
*      ALWAYS FORMAT THE HDD WITH THE SAME VERSION CONTROLLER         *
*      BOARD AND HDC CPU FIRMWARE VERSION IT WILL BE USED WITH.       *
*      IT IS NOT NECESSARY TO REFORMAT IF THE ROM BIOS IS             *
*      UPGRADED AS LONG AS THE SAME FIRMWARE CPU IS USED.             *
*                                                                     *
***********************************************************************
```

FOR LOW LEVEL FORMATTING:

1. EQUITY I/II FORMAT
   See PSB # S-0005 titled Equity I/II HDD intialization procedure using software which is included with each system.

2. EQUITY III FORMAT
   a. Run PFORMAT - Enter bad tracks - Time approx. 5 minutes.
   b. Run HDFMTALL - Time approx. 8 minutes.
   c. Run HDPART - Time approx. 2 minutes.
   d. Run HDFORMAT - Time approx. 5 minutes.

3. EQUITY III+ - See Product Support Bulletin # S-0006

Notes:

1. Early production Equity I units without HDDs must be upgraded with the CAC version VFO SUB-board to operate with a hard drive.
2. Equity I, DOS ver. 2.11 problem - Bad sector information erased when HDFORMAT (MS-DOS utility) executes formatting. Corrected in DOS version 2.2 (MSA-B3) and 2.21 (MSA-B4).
3. Equity I/II - HDFMTALL erases bad sector information. Delete HDFMTALL from the system disk.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 4/7/87 NUMBER: S-0010
SUBJECT: EQUITY I+ / EQUITY III+ WORLDWIDE POWER SELECTION

The purpose of this bulletin is to caution you on the use of the 115/230 VAC power selection on the Equity I+ and Equity III+ personal computer.

The new Equity I+ and Equity III+ personal computers have the capability of operating both in the U.S.A. and internationally through a switch selectable 115/230 Volt, 60/50Hz power supply.

Both Equity units have a separate A.C. outlet on the rear panel for providing AC power to a peripheral device (usually a monitor). The power is controlled by the system unit on/off switch.

It is very important that you inform users who intend to use the system internationally, that any peripheral device which is connected to this outlet must be configured to operate on the same input voltage that is supplied to the Equity system unit.

In other words, you must not connect a peripheral device which requires 115 VAC to the rear panel outlet if the input voltage to the Equity system is 230 Volts or serious electrical damage to the peripheral device may occur.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 6/8/87 NUMBER: S-0011
SUBJECT: MS-DOS 3.2 SELECT COMMAND - MANUAL ERROR

A documentation error has been identified in the MS-DOS version 3.2 manual which is supplied with the Equity I+ and III+, there is an error in the documentation for the SELECT command. This error also occurs in the HELP utility data file.

In the respective sections on using the Equity hard disk drive, the syntax is given as:

SELECT C: 001 US

Also, in the HELP utility, the format is given as:

SELECT [DOS source d:] [target d:] xxx yy

with the square brackets indicating optional command line parameters. This turns out not to be the case; both source and destination drives are required parameters.

So - there are two solutions. One is to use the "traditional" method for logical formatting:

FORMAT C: /S/V

or use the correct SELECT syntax:

SELECT A: C: 001 US

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 6/8/87 NUMBER: S-0012
SUBJECT: EPSON EQUITY ENHANCED KEYBOARD COMPATIBILITY

The purpose of this bulletin is to provide information regarding the compatibility of the enhanced "AT" style Equity Plus series keyboard with the Equity family of computers and a general statement on software support.

With the introduction of the Equity I+ and III+, Epson brought out an enhanced keyboard design - very similar to the enhanced keyboard introduced by IBM on the Model 339 AT. There are a couple of areas to make note of.

1. Keyboard Compatibility

   The enhanced keyboard cannot be used on an Equity I, II or III. The enhanced keyboard (as with IBM's) requires explicit ROM BIOS support. The Equity I+ and Equity III+ incorporate this support; the earlier machines do not.

   It is possible, however, to use a third-party "enhanced-style" keyboard (such as the Datadesk Turbo-101) which offers switch selection for PC/XT or AT usage. (Please note that early versions of the Equity I and II did not support any third party keyboards.)

   The correct jumper settings for non-Epson keyboards are:

Equity I:	J2 and J3 jumpered
Equity II:	J3, J4 and J5 set for position 1

   Also note that once the above jumper changes have been made, attempting to use the Epson keyboard will result in damage to the keyboard and main board.

2. Software Compatibility

   Not all applications "know" about the enhanced keyboard. The scan codes and mapping are subtly different. If you experience difficulties with certain applications (particularly any that re-program the keyboard), contact the software vendor and ask about enhanced keyboard support.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 7/29/87 NUMBER: S-0015A
SUBJECT: EPSON HD-860 HARD DISK DRIVE WARRANTY EXTENSION

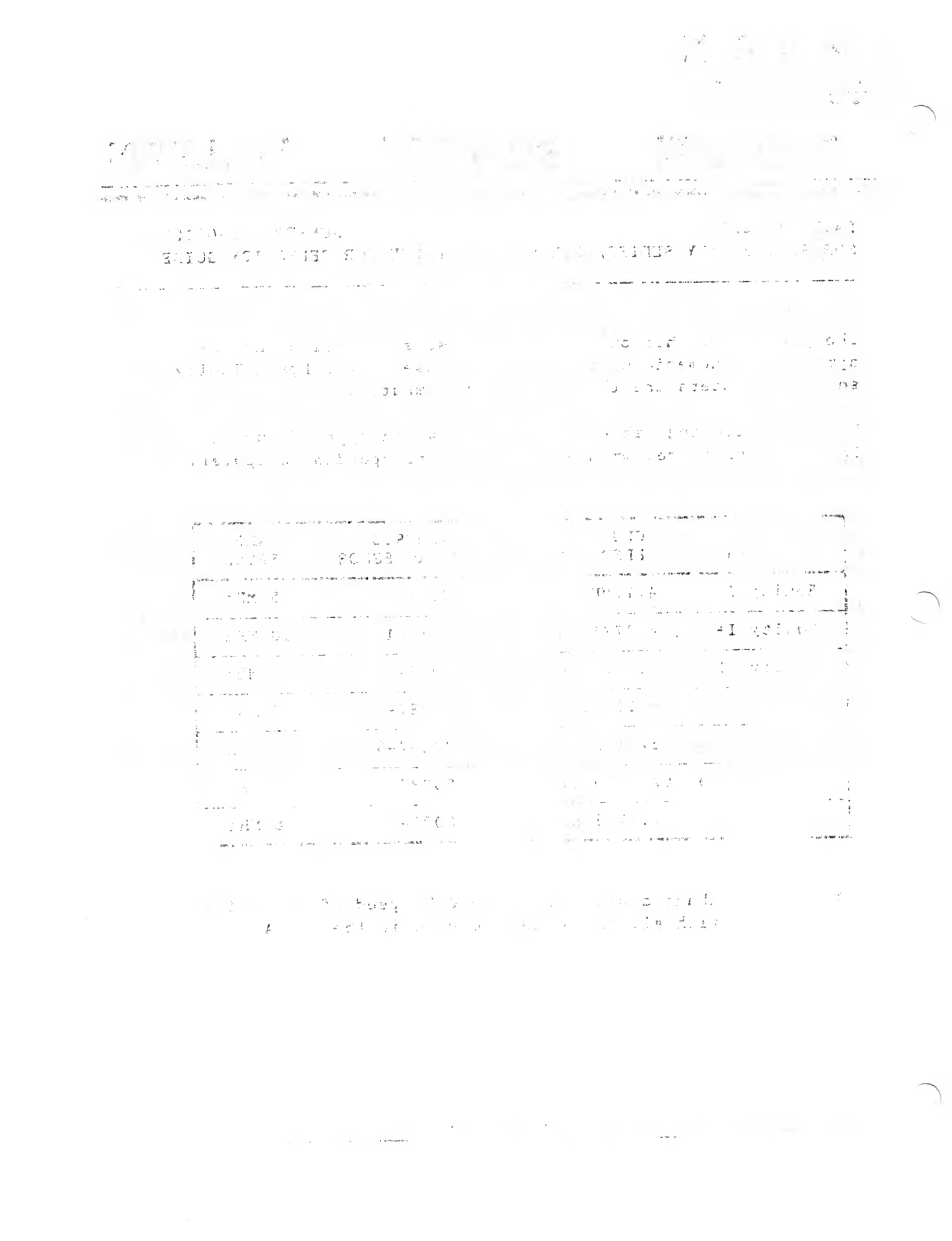
The purpose of this bulletin is to inform you of a change in the warranty period for the HD-860 hard disk drive unit.

Epson America, Inc. has made the decision to extend the warranty period for the HD-860 hard disk drive, installed in the Equity product line, for an indefinite period. This warranty extension will cover all HD-860 hard disk drives regardless of the purchase date. Standard warranty claim procedures are to be followed for these failures. The normal warranty labor reimbursement and no charge parts exchange will be given for these claims.

This warranty extension is for HD-860 failures only and Epson America, Inc. reserves the right to cancel this HD-860 warranty extension at any time. It is designed to promote the satisfaction of our mutually inclusive customer base with the Epson products.

Epson's Service Department is currently providing HMD-720 hard disk drive units as warranty replacements for returned HD-860's. Authorized Service Centers and Customer Care Centers should not use HD-860's as repair replacements. Any ASC or CCC having HD-860's in repair float stock may exchange these for HMD-720's by contacting Warranty Administration for an RMA.

Note: <u>This exchange does not apply to sales product</u>, and is contingent upon availability of Epson's float exchange stock.



EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/2/87 NUMBER: S-0019B
SUBJECT: EQUITY SERIES/APEX MATH CO-PROCESSOR SELECTION GUIDE

The purpose of this bulletin is to assist in selecting the appropriate numeric co-processor for use in the Epson Equity series computers and the Epson Apex computer.

Use the following table to determine which type of Numeric Co-Processor is recommended for the corresponding computer.

EPSON COMPUTER	CPU SPEED	NUMERIC CO-PROCESSOR	NXP SPEED
Equity I	4.77MHz	8087	5 MHz
Equity I+	4.77/10MHz	8087-1	10 MHz
Equity II	4.77/7.16MHz	8087-2	8 MHz
Equity II+	8/10MHz	80287-8	8 MHz
Equity III	6/8MHz	80287-6	6 MHz
Equity III+	6/8/(10/12)MHz*	80287-8	8 MHz
Apex	4.77/8MHz	8087-2	8 MHz

* Product enhanced with increased CPU speed of 6/8/12Mhz starting with all units manufactured in the U.S.A..

Quarterly Sales Report

Item	Quantity	Price
Widget A	1,250	$4.99
Widget B	3,400	$7.50
Gadget X	875	$12.00
Gadget Y	2,100	$3.25
Sprocket	5,000	$0.75
Flange	1,600	$2.40
Bracket	950	$6.10
Coupling	4,200	$1.85

EPSON

EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 11/19/87 **NUMBER:** S-0026
SUBJECT: Equity + Series Compatibility Certification

The following products have been certified for compatiblity with the Equity + series computers:

Hard Disk Controllers

Manufacturer	Model#	Type	For use in
Western Digital	1002B-WX1	MFM	EQ I+
Western Digital	1003B-WAH	MFM	EQ II+, EQ III+
IBM	Enhanced AT	MFM	EQ II+, EQ III+
DTC	5160-CRH	RLL	EQ II+, EQ III+
Western Digital	WD1003-WA2	MFM	EQ II+, EQ III+
Western Digital	1002-27X	RLL	EQ II+, EQ III+

Hard Drives

Manufacturer	Model	Type	For use in
Epson	HMD-720	MFM	EQ I+, EQ II+, EQ III+
CDC-Wren II	94205-51	MFM	EQ II+, EQ III+
Miniscribe	6053	MFM	EQ III+
Miniscribe	8438F	RLL	EQ II+, EQ III+

Memory Expansion Boards

Manufacturer	Model	For use in
AST Research	Advantage Premium	EQ II+, EQ III+
AST Research	Rampage 286	EQ II+, EQ III+
Intel Corp.	Aboveboard	EQ II+, EQ III+
Intel Corp.	Aboveboard 286 p/s	EQ II+, EQ III+
STB Systems	Grande Byte	EQ II+, EQ III+
STB Systems	Rio Grande	EQ II+, EQ III+
Profit Systems	Elite 16	EQ II+, EQ III+

[illegible] SUPPORT [illegible]

[illegible] Apple® Users with Microsoft® and Star® Printers

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PRODUCT SUPPORT BULLETIN

DATE: 12/14/87 NUMBER: S-0031
SUBJECT: Equity Series with Microsoft Word and Serial Printers

This bulletin is to inform you of a potential problem when using Microsoft Word, certain Equity computers and a serial printer. The situation exists on:

Equity I	BIOS rev. 2.21 or earlier
Equity I+	BIOS rev. 1.02
Equity II+	BIOS rev. 2.00
Equity III+ (10 MHz)	BIOS rev. 1.50 or earlier
Equity III+ (12 MHz)	BIOS rev. 2.00
Apex	BIOS rev. 1.00

When Word is configured to drive a serial printer via COM1 or COM2, it will print a character every 1 to 2 seconds. A single line of text may take up to a minute to print.
Word uses BIOS interrupt 14h (serial output) function 1 (send character to port) for driving either COM port. The function number is placed in the AH register and the interrupt called. On return, AH is supposed to contain the line control status. However, AH is still set to 1, indicating that a character is ready to be received. Word then calls interrupt 14h, function 2 (receive character) and attempts to receive the character. After 1 to 2 seconds, the routine times out and transmission is resumed.

There are three methods of correcting this situation:

1) If the printer supports hardware handshaking, redirect the printer output (MODE LPT1:=COM1:) and configure Word for LPT1. This works reliably with Epson printers or similar devices.

2) Epson has developed a patch program (SERFIX.COM). This is a TSR that insures that proper status is returned from INT 14h, function 1. This program is available from CompuServe (Epson and Microsoft Forums) and the Product Support Center BBS.

3) A revised ROM BIOS has been developed for the above systems. This is a limited release and will only be supplied on an as-needed basis.

Method 1 is the easiest solution. Method 2 is effective and is recommended for individual users. Method 3 should be reserved for large, multi-unit upgrades on an as-needed basis.

Please contact the Systems Support Group if you need additional information.

FILE NO.:
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AUTHORIZED BY:

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TECHNICAL INFORMATION BULLETIN

TIB NO.: HD860-002
DATE: 9/28/87
PAGE (s): 1 of 1
SUBMITTED BY: Bob Merchant
AUTHORIZED BY: L. Hlapple

MACHINE (s): HD-860

REFERENCE: N/A

TITLE: EPSON HD-860 HARD DISK DRIVE WARRANTY EXTENSION

The purpose of this bulletin is to inform you of a change in the warranty period for the HD-860 hard disk drive unit.

Epson America, Inc. has made the decision to extend the warranty period for the HD-860 hard disk drive, installed in the Equity product line, for an indefinite period. This warranty extension will cover all HD-860 hard disk drives regardless of the purchase date. Standard warranty claim procedures are to be followed for these failures. The normal warranty labor reimbursement and no charge parts exchange will be given for these claims.

This warranty claim extension is for HD-860 failures only and Epson America, Inc. reserves the right to cancel this HD-860 warranty extension at any time. It is designed to promote the satisfaction of our mutually inclusive customer base with Epson products.

Epson Service Department is currently providing HMD-720 hard disk drive units as warranty replacements for returned HD-860's. Authorized Service Centers and Customer Care Centers should not use HD-860's as repair replacements. Any ASC or CCC having HD-860's in repair float stock may exchange these for HMD-720's by contacting Warranty Administration for an RMA.

Note: <u>This exchange does not apply to sales product</u>, and is contingent upon availability of Epson's float exchange stock.